12-Bit, 6 GSPS/10.25 GSPS, JESD204B, RF Analog-to-Digital Converter

Data Sheet

AD9213

FEATURES

High instantaneous dynamic range
NSD
- **−155 dBFS/Hz at 10 GSPS with −9 dBFS, 170 MHz input**
- **−153 dBFS/Hz at 10 GSPS with −1 dBFS, 170 MHz input**

SFDR: 70 dBFS at 10 GSPS with −1 dBFS, 1000 MHz input
SFDR excluding H2 and H3 (worst other spur): 89 dBFS at 10 GSPS with −1 dBFS, 1000 MHz input
Low power dissipation: <4.6 W typical at 10 GSPS
Integrated input buffer (6.5 GHz input bandwidth)
- **1.4 V p-p full-scale analog input with R_{IN} = 50 Ω**
- **Overvoltage protection**

16-lane JESD204B output (up to 16 Gbps line rate)
Multichip synchronization capable with 1 sample accuracy
- **DDC NCO synchronization included**

Integrated DDC
- **Selectable decimation factors**
- **16 profile settings for fast frequency hopping**

Fast overrange detection for efficient AGC
On-chip temperature sensor
On-chip negative voltage generators
Low CER: <1 × 10^{-16}
12 mm × 12 mm, 192-ball BGA-ED package

GENERAL DESCRIPTION

The AD9213 is a single, 12-bit, 6 GSPS/10.25 GSPS, radio frequency (RF) analog-to-digital converter (ADC) with a 6.5 GHz input bandwidth. The AD9213 supports high dynamic range frequency and time domain applications requiring wide instantaneous bandwidth and low conversion error rates (CER).

The AD9213 features a 16-lane JESD204B interface to support maximum bandwidth capability.

The AD9213 achieves dynamic range and linearity performance while consuming <4.6 W typical. The device is based on an interleaved pipeline architecture and features a proprietary calibration and randomization technique that suppresses interleaving spurious artifacts into its noise floor. The linearity performance of the AD9213 is preserved by a combination of on-chip dithering and calibration, which results in excellent spurious-free performance over a wide range of input signal conditions.

Applications that require less instantaneous bandwidth can benefit from the on-chip, digital signal processing (DSP) capability of the AD9213 that reduces the output data rate along with the number of JESD204B lanes required to support the device. The DSP path includes a digital downconverter (DDC) with a 48-bit, numerically controlled oscillator (NCO), followed by an I/Q digital decimator stage that allows selectable decimation rates that are factors of two or three. For fast frequency hopping applications, the AD9213 NCO supports up to 16 profile settings with a separate trigger input, allowing wide surveillance frequency coverage at a reduced JESD204B lane count.

The AD9213 supports sample accurate multichip synchronization that includes synchronization of the NCOs. The AD9213 is offered in a 192-ball ball grid array (BGA) package and is specified over a junction temperature range of −20°C to +115°C.

FUNCTIONAL BLOCK DIAGRAM

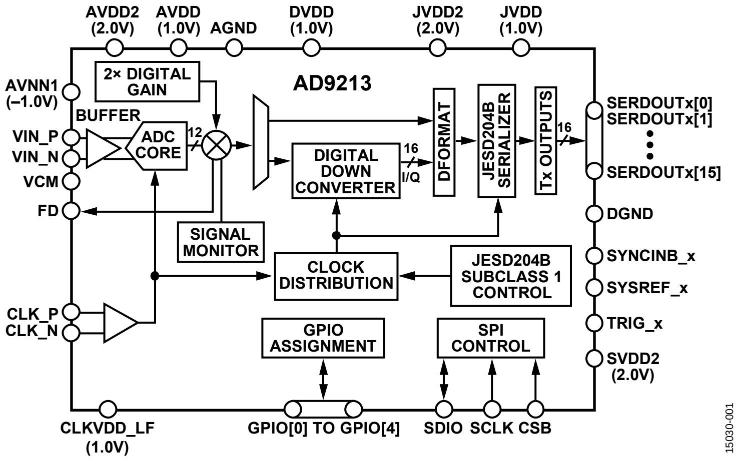

Figure 1.

Rev. A Document Feedback

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8/2019—Revision 0: Initial Version

SPECIFICATIONS

Nominal supply voltages, specified maximum sampling rate, internal reference, analog input (A_{IN}) = −1.0 dBFS. Minimum/maximum specifications represent performance at −20°C ≤ T_J ≤ +115°C, unless otherwise noted. Typical specifications represent performance at T_J = 70°C.

Table 1.

	AD9213-6G			AD9213-10G			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	12			12			Bits
ACCURACY							
No Missing Codes		Guaranteed			Guaranteed		
Offset Error	−10	−0.6	+9	−11	0	+11	LSB
Gain Error	−3.1	11.1	+19.2	−7.0	7.4	+17.0	%FSR
Differential Nonlinearity (DNL)	−0.5	±0.25	+0.5	−0.5	±0.3	+0.6	LSB
Integral Nonlinearity (INL)	−4.8	±0.7	+7.4	−8.2	±2.4	+6.2	LSB
ANALOG INPUTS							
Differential Input Voltage Range (Internal V_{REF} = 0.5 V)		1.4			1.4		V p-p
Resistance (R_{IN})	47.8	50	52.2	47.8	50.0	52.2	Ω
Capacitance		1			1		pF
Internal Common-Mode Voltage (V_{CM})		0.5			0.5		V
Analog Full Power Bandwidth (Internal Termination)		6.5			6.5		GHz
Input Referred Noise		1.61			1.72		LSB_{RMS}
POWER SUPPLIES							
BVDD2	1.95	2.0	2.05	1.95	2.0	2.05	V
BVNN1	−1.025	−1.0	−0.975	−1.025	−1.0	−0.975	V
AVNN1	−1.025	−1.0	−0.975	−1.025	−1.0	−0.975	V
BVNN2 (Internally Generated)	−2.05	−2.0	−1.95	−2.05	−2.0	−1.95	V
BVDD3 (Internally Generated)	2.925	3.0	3.075	2.925	3.0	3.075	V
AVDD	0.975	1.0	1.025	0.975	1.0	1.025	V
CLKVDD_LF	0.975	1.0	1.025	0.975	1.0	1.025	V
PLLVDD2	1.95	2.0	2.05	1.95	2.0	2.05	V
AVDDFS8	0.975	1.0	1.025	0.975	1.0	1.025	V
FVDD	0.975	1.0	1.025	0.975	1.0	1.025	V
VDD_NVG	0.975	1.0	1.025	0.975	1.0	1.025	V
RVDD2	1.95	2.0	2.05	1.95	2.0	2.05	V
SVDD2	1.75	2.0	2.05	1.75	2.0	2.05	V
JVDD2	1.95	2.0	2.05	1.95	2.0	2.05	V
DVDD	0.975	1.0	1.025	0.975	1.0	1.025	V
JVTT	0.975	1.0	1.025	0.975	1.0	1.025	V
JVDD	0.975	1.0	1.025	0.975	1.0	1.025	V
TMU_AVDD2	1.95	2.0	2.05	1.95	2.0	2.05	V
TMU_DVDD1	0.975	1.0	1.025	0.975	1.0	1.025	V
I_{BVDD2}		109	143		112	147	mA
I_{BVNN1}		−115	−149		−116	−151	mA
I_{AVNN1}		−1.8	−2.1		−1.8	−2	mA
I_{BVNN2}[1]	N/A[2]	N/A[2]	N/A[2]	N/A[2]	N/A[2]	N/A[2]	mA
I_{BVDD3}[1]	N/A[2]	N/A[2]	N/A[2]	N/A[2]	N/A[2]	N/A[2]	mA
I_{AVDD}		1730	2240		2180	2790	mA
I_{CLKVDD_LF}		28	34		31	37	mA
$I_{PLLVDD2}$		1	2		1	2	mA
$I_{AVDDFS8}$		26	44		38	56	mA
I_{FVDD}		25	28		31	35	mA
I_{VDD_NVG}[3]		155	193		159	195	mA
I_{VDD_NVG}[4]		383	479		387	478	mA
I_{RVDD2}		32	35		35	38	mA
I_{SVDD2}		0.3	1		0.3	1	mA

	AD9213-6G			AD9213-10G			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{JVDD2}		27	32		21	24	mA
I_{DVDD}[5]		400	770		643	1055	mA
I_{JVTT}		146	235		173	247	mA
I_{JVDD}		387	564		611	800	mA
I_{TMU_AVDD2}		1.7	2		1.7	2	mA
I_{TMU_DVDD1}		0.25	1		1	2	mA
Power Consumption[6]							
Total Power Dissipation (Including Output Drivers)[7]		3.47	4.83		4.44	5.93	W
Power-Down		114			114		mW
Standby		2.7			2.7		W

[1] Internally supplied.
[2] N/A means not applicable.
[3] Current when AVNN1 and BVNN1 are supplied by an external source.
[4] Current when AVNN1 and BVNN1 are supplied by VNEG_OUT.
[5] DDC off.
[6] Power with optional DDC off. Power and supply currents are typical unless otherwise noted.
[7] Total power when AVNN1 and BVNN1 are supplied by VNEG_OUT.

AC SPECIFICATIONS

Nominal supply voltages, specified maximum sampling rate, internal reference, A_{IN} = −1.0 dBFS. Minimum/maximum specifications represent performance at −20°C ≤ T_J ≤ +115°C, unless otherwise noted. Typical specifications represent performance at T_J = 70°C.

Table 2.

	AD9213-6G			AD9213-10G			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
NOISE SPECTRAL DENSITY (NSD)							
At 170 MHz, −1 dBFS		−153			−153		dBFS/Hz
At 170 MHz, −9 dBFS		−153.8			−155.1		dBFS/Hz
At 170 MHz, −30 dBFS		−153.9			−155.7		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)							
Input Frequency (f_{IN}) = 170 MHz		58.2			55.9		dBFS
f_{IN} = 1000 MHz		56.8			55.8		dBFS
f_{IN} = 2600 MHz	50.1	52.3		43.8	51.0		dBFS
f_{IN} = 4000 MHz		50.2			49.9		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)							
f_{IN} = 170 MHz		58.2			55.6		dBFS
f_{IN} = 1000 MHz		56.6			55.6		dBFS
f_{IN} = 2600 MHz	48.8	52.3		42.7	50.8		dBFS
f_{IN} = 4000 MHz		49.3			49.4		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)							
f_{IN} = 170 MHz		9.4			8.9		Bits
f_{IN} = 1000 MHz		9.1			8.9		Bits
f_{IN} = 2600 MHz		8.4			8.1		Bits
f_{IN} = 4000 MHz		7.9			7.9		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR), SECOND OR THIRD HARMONIC							
f_{IN} = 170 MHz		81			70		dBFS
f_{IN} = 1000 MHz		71			70		dBFS
f_{IN} = 2600 MHz	60	76		62	65		dBFS
f_{IN} = 4000 MHz		57			60		dBFS
SECOND HARMONIC (H2)							
f_{IN} = 170 MHz		−90			−71		dBFS
f_{IN} = 1000 MHz		−89			−77		dBFS
f_{IN} = 2600 MHz		−76	-60		−65	−62	dBFS
f_{IN} = 4000 MHz		−57			−60		dBFS

Parameter	AD9213-6G			AD9213-10G			Unit
	Min	Typ	Max	Min	Typ	Max	
THIRD HARMONIC (H3)							
f_{IN} = 170 MHz		−81			−70		dBFS
f_{IN} = 1000 MHz		−71			−70		dBFS
f_{IN} = 2600 MHz		−76	−66		−72	−65	dBFS
f_{IN} = 4000 MHz		−67			−74		dBFS
WORST OTHER (WO), EXCLUDING SECOND OR THIRD HARMONIC (|WO| = SFDR EXCLUDING H2 OR H3)							
f_{IN} = 170 MHz		−89			−88		dBFS
f_{IN} = 1000 MHz		−95			−89		dBFS
f_{IN} = 2600 MHz		−85	−76		−89	−72	dBFS
f_{IN} = 4000 MHz		−82			−86		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD3, $2f_{IN1} - f_{IN2}$) f_{IN1} AND f_{IN2} = −7.0 dBFS							
f_{IN1} = 1842 MHz, f_{IN2} = 1847 MHz		−80			−77		dBFS
f_{IN1} = 2138 MHz, f_{IN2} = 2143 MHz		−75			−76		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD3, $2f_{IN1} - f_{IN2}$) f_{IN1} AND f_{IN2} = −15.0 dBFS							
f_{IN1} = 1842 MHz, f_{IN2} = 1847 MHz		−108			−99		dBFS
f_{IN1} = 2138 MHz, f_{IN2} = 2143 MHz		−100			−101		dBFS

DIGITAL SPECIFICATIONS

Nominal supply voltages, specified maximum sampling rate, internal reference, A_{IN} = −1.0 dBFS. Minimum/maximum specifications represent performance at $-20°C \le T_J \le +115°C$, unless otherwise noted. Typical specifications represent performance at T_J = 70°C.

Table 3.

Parameter	Min	Typ	Max	Unit
CLOCK INPUTS (CLK_P, CLK_N)				
Logic Compliance		Low voltage positive emitter coupled logic (LVPECL)		
Differential Input Voltage	300	800	1800	mV p-p
Common-Mode Input Voltage		0.675		V
Input Resistance (Differential)		106		Ω
Input Capacitance		0.9		pF
SYSREF_x INPUTS				
Logic Compliance		LVDS		
Differential Input Voltage	500	700	800	mV p-p
Common-Mode Input Voltage		1.2		V
Input Resistance (Differential)		100		Ω
Input Capacitance		0.5		pF
LOGIC INPUTS (SDIO, SCLK, CSB, GPIO, PWDN)				
Logic Compliance		Complementary metal-oxide semiconductor (CMOS)		
Voltage				
Logic 1	0.70 × SVDD2			V
Logic 0	0		0.30 × SVDD2	V
Input Resistance (Single-Ended)		44		kΩ
SYNCINB_x INPUT				
Logic Compliance		LVDS		
Input Voltage	400	800	1800	
Differential				mV p-p
Common Mode		0.675	2.0	V
Input Resistance (Differential)		18		kΩ
Input Capacitance		1		pF

Parameter	Min	Typ	Max	Unit
LOGIC OUTPUT (SDIO, GPIO, FD)				
Logic Compliance		CMOS		
Voltage				
Logic 1, Output Logic Current High (I_{OH}) = 4 mA	SVDD2 − 0.45			V
Logic 0, Output Logic Current Low (I_{OL}) = 4 mA	0		0.45	V
RESET (RSTB) INPUT				
Logic Compliance		CMOS		
Voltage				
Logic 1	0.70 × SVDD2			V
Logic 0	0		0.30 × SVDD2	V
Input Resistance		77		kΩ

SWITCHING SPECIFICATIONS

Nominal supply voltages, specified maximum sampling rate, internal reference, AIN = −1.0 dBFS. Minimum/maximum specifications represent performance at −20°C ≤ T_J ≤ +115°C, unless otherwise noted. Typical specifications represent performance at T_J = 70°C.

Table 4.

Parameter	Min	Typ	Max	Unit
CLOCK (CLK)				
Maximum Clock Rate			10.25	GSPS
Minimum Clock Rate	2.5			GSPS
Clock Duty Cycle	45	50	55	% duty cycle
LATENCY				
Pipeline Latency		367		Clock cycles
Fast Detect Latency (FD)		170		Clock cycles
OUTPUT PARAMETERS (SERDOUT_x[x], x = 0 to 15)				
Logic Compliance		JESD204B		
Differential Output Voltage	560	770		mV p-p
Differential Termination Impedance	100	120		Ω
Unit Interval (UI)[1]	62.5	80	588.2	ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)		26		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)		26		ps
Phase-Locked Loop (PLL) Lock Time		5		ms
Lane Rate (Nonreturn to Zero)[2]	1.7	12.5	16	Gbps
WAKE-UP TIME				
Standby		1		ms
Power-Down		25		ms
APERTURE				
Delay (t_A)		120		ps
Uncertainty (Jitter, t_J)		50		(f_S) rms

[1] Baud rate = 1/UI. A subset of this range can be supported.
[2] Default L = 16. This number can be changed based on the sample rate and decimation ratio.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYSREF_x TIMING REQUIREMENTS[1]					
t_{SU_SR}	Device clock to SYSREF_P setup time		−65		ps
t_{H_SR}	Device clock to SYSREF_P hold time		95		ps
SERIAL PORT INTERFACE (SPI) TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	4			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	4			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK can be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK can be in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the CSB rising edge (not shown in Figure 3)	10			ns

[1] SYSREF_x setup and hold times are defined with respect to the rising SYSREF_x edge and rising clock edge. Positive setup time leads the clock edge. Negative hold time also leads the clock edge. There are no SYSREF_x setup and hold requirements in averaged SYSREF_x mode, which is the primary JESD204B Subclass 1 mode for the AD9213.

Timing Diagrams

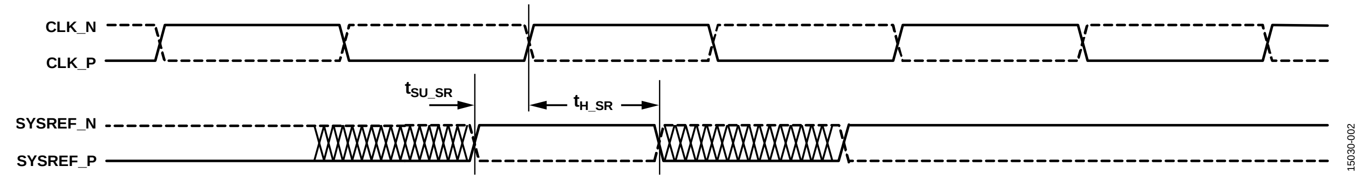


Figure 2. SYSREF_x Setup and Hold Timing Diagram

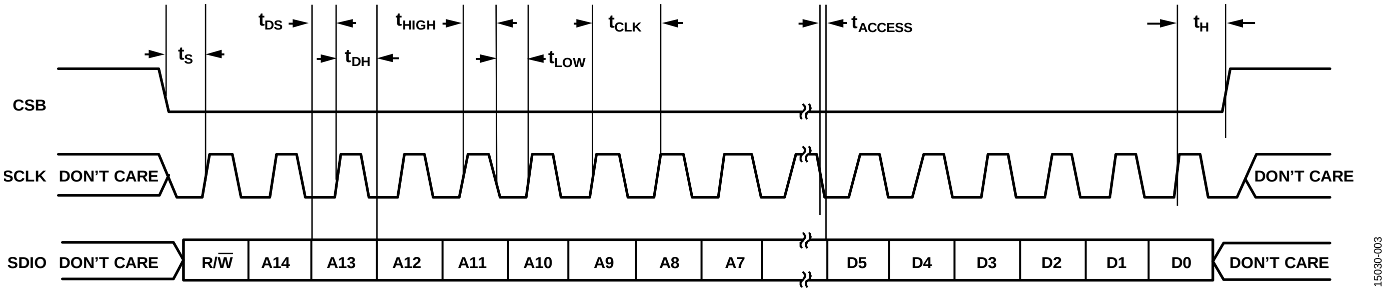


Figure 3. Serial Port Interface Timing Diagram (MSB First)

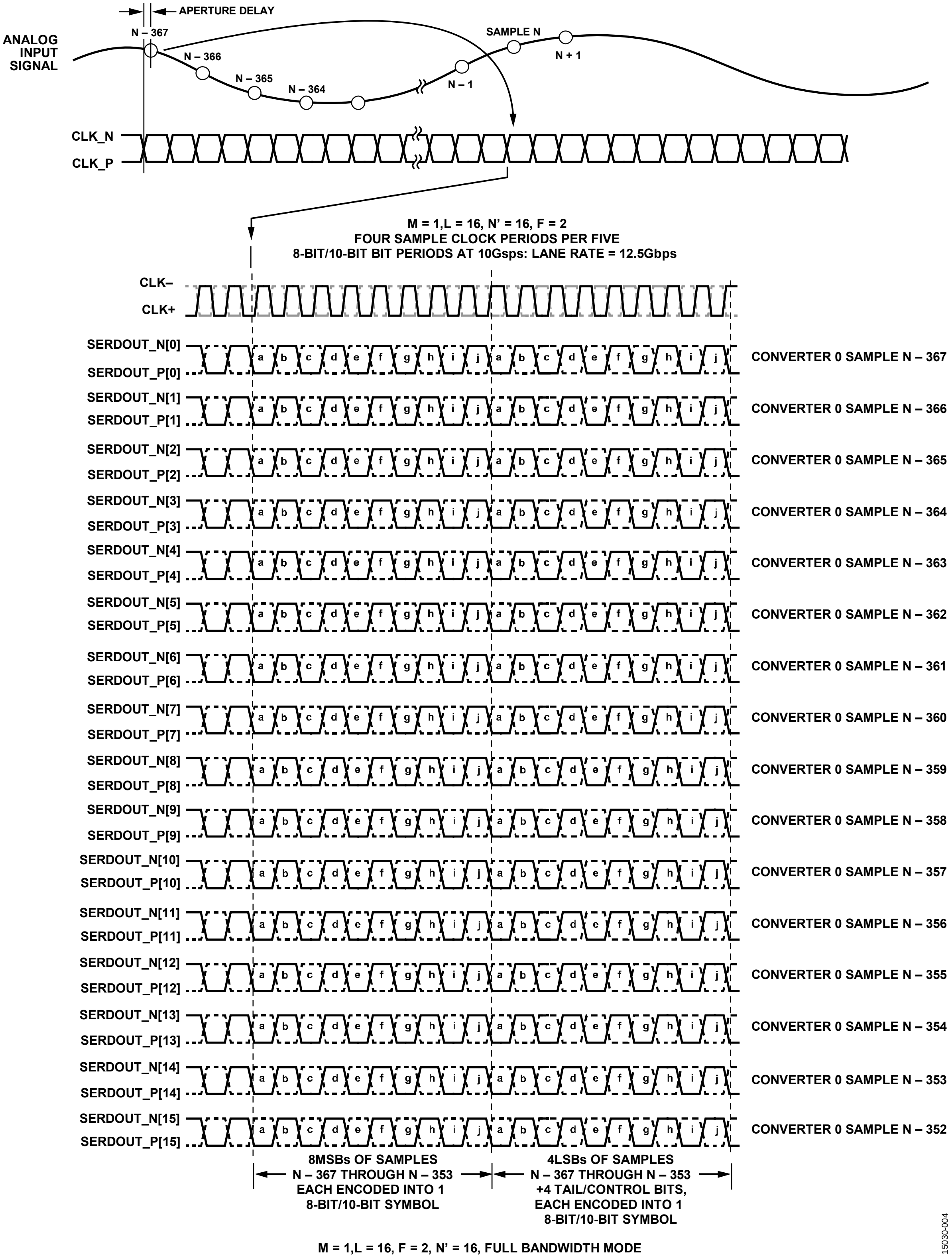


Figure 4. Data Output Timing for 16-Lane Mode

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Supply Pins	
BVDD2 to AGND	2.2 V
BVNN1 to AGND	−1.1 V
AVNN1 to GND	−1.1 V
AVDD to AGND	1.1 V
CLKVDD_LF to AGND	1.1 V
PLLVDD2 to AGND	2.2 V
AVDDFS8 to AVSSFS8	1.1 V
FVDD to AGND	1.1 V
VDD_NVG to VSS_NVG	1.1 V
RVDD2 to AGND	2.2 V
SVDD2 to DGND	2.2 V
DVDD to DGND	1.1 V
JVTT to JGND	1.1 V
JVDD to JGND	1.1 V
JVDD2 to JGND	2.2 V
TMU_AVDD2 to AGND	2.2 V
TMU_DVDD1 to AGND	1.1 V
GND Pins	
AVSSFS8 to DGND	−0.3 V to +0.3 V
VSS_NVG to DGND	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
AGND to JGND	−0.3 V to +0.3 V
DGND to JGND	−0.3 V to +0.3 V
Input/Output Pins	
VIN_x to AGND	−0.125 V to AVDD + 0.150 V
CLK_x to AGND	AGND − 0.3 V to CLKVDD_LF + 0.3 V
CSB, RSTB, PDWN, SCLK, FD, GPIO[x], SDIO to DGND	DGND − 0.3 V to SVDD2 + 0.3 V
SYNCINB_x to DGND	DGND − 0.3 V to DVDD + 0.3 V
SYSREF_x, TRIG_x to AVSSFS8	1.8 V
TMU_REFx to TMU_AGND	AGND − 0.3 V to TMU_AVDD2 + 0.3 V
VCM to AGND	AGND − 0.3 V to RVDD2 + 0.3 V
VREF to AGND	AGND − 0.3 V to RVDD2 + 0.3 V
SERDOUT_x[x] to JGND	JGND − 0.3 V to JVTT + 0.3 V
Storage Temperature, T_A	−40°C to +150°C
Operating Junction Temperature (T_J)	125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

θ_{JB} is the junction to board thermal resistance.

Table 7. Thermal Resistance

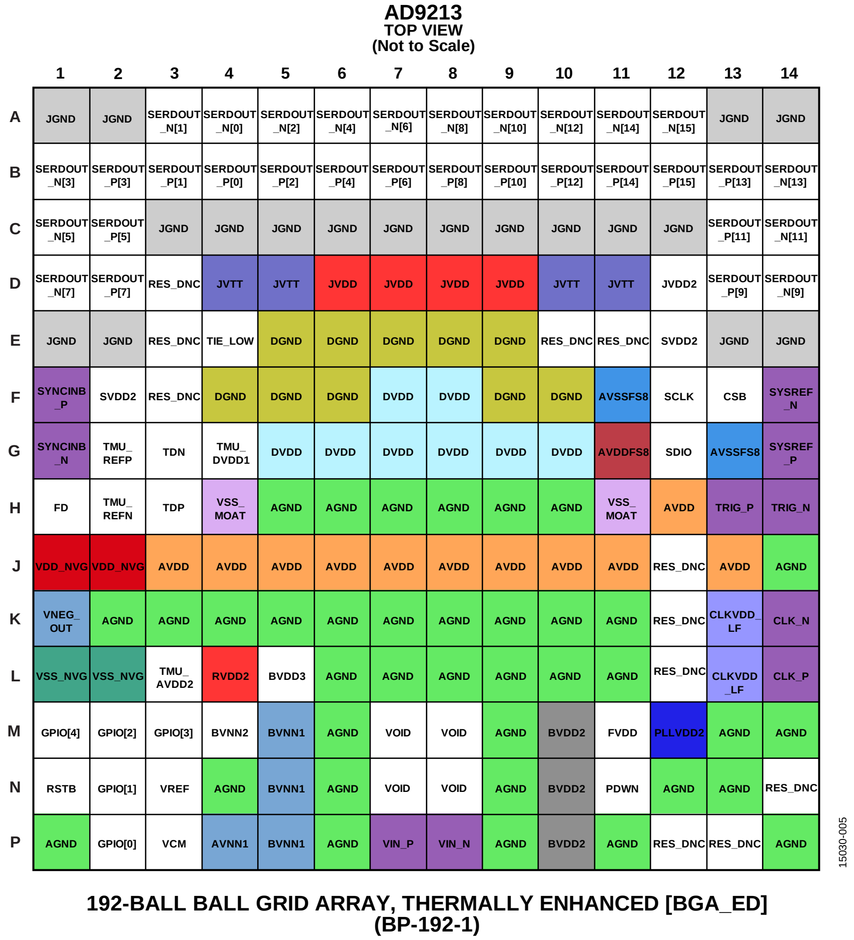
Package Type	θ_{JA}	θ_{JC}	θ_{JB}	Unit
BP-192-1	20.5	1.6	9.2	°C/W

[1] Thermal resistance values specified are simulated based on JEDEC specs in compliance with JESD51-12.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



AD9213
TOP VIEW
(Not to Scale)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	JGND	JGND	SERDOUT _N[1]	SERDOUT _N[0]	SERDOUT _N[2]	SERDOUT _N[4]	SERDOUT _N[6]	SERDOUT _N[8]	SERDOUT _N[10]	SERDOUT _N[12]	SERDOUT _N[14]	SERDOUT _N[15]	JGND	JGND
B	SERDOUT _N[3]	SERDOUT _P[3]	SERDOUT _P[1]	SERDOUT _P[0]	SERDOUT _P[2]	SERDOUT _P[4]	SERDOUT _P[6]	SERDOUT _P[8]	SERDOUT _P[10]	SERDOUT _P[12]	SERDOUT _P[14]	SERDOUT _P[15]	SERDOUT _P[13]	SERDOUT _N[13]
C	SERDOUT _N[5]	SERDOUT _P[5]	JGND	JGND	JGND	JGND	JGND	JGND	JGND	JGND	JGND	JGND	SERDOUT _P[11]	SERDOUT _N[11]
D	SERDOUT _N[7]	SERDOUT _P[7]	RES_DNC	JVTT	JVTT	JVDD	JVDD	JVDD	JVDD	JVTT	JVTT	JVDD2	SERDOUT _P[9]	SERDOUT _N[9]
E	JGND	JGND	RES_DNC	TIE_LOW	DGND	DGND	DGND	DGND	DGND	RES_DNC	RES_DNC	SVDD2	JGND	JGND
F	SYNCINB _P	SVDD2	RES_DNC	DGND	DGND	DGND	DVDD	DVDD	DGND	DGND	AVSSFS8	SCLK	CSB	SYSREF _N
G	SYNCINB _N	TMU_ REFP	TDN	TMU_ DVDD1	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDDFS8	SDIO	AVSSFS8	SYSREF _P
H	FD	TMU_ REFN	TDP	VSS_ MOAT	AGND	AGND	AGND	AGND	AGND	AGND	VSS_ MOAT	AVDD	TRIG_P	TRIG_N
J	VDD_NVG	VDD_NVG	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	RES_DNC	AVDD	AGND
K	VNEG_ OUT	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	RES_DNC	CLKVDD_ LF	CLK_N
L	VSS_NVG	VSS_NVG	TMU_ AVDD2	RVDD2	BVDD3	AGND	AGND	AGND	AGND	AGND	AGND	RES_DNC	CLKVDD _LF	CLK_P
M	GPIO[4]	GPIO[2]	GPIO[3]	BVNN2	BVNN1	AGND	VOID	VOID	AGND	BVDD2	FVDD	PLLVDD2	AGND	AGND
N	RSTB	GPIO[1]	VREF	AGND	BVNN1	AGND	VOID	VOID	AGND	BVDD2	PDWN	AGND	AGND	RES_DNC
P	AGND	GPIO[0]	VCM	AVNN1	BVNN1	AGND	VIN_P	VIN_N	AGND	BVDD2	AGND	RES_DNC	RES_DNC	AGND

192-BALL BALL GRID ARRAY, THERMALLY ENHANCED [BGA_ED]
(BP-192-1)

Figure 5. Pin Configuration (Top View, Not To Scale)

Table 8. Pin Function Descriptions

Pin No.	Ball Mnemonic	Ball Type	Signal Type	Description
A1, A2, A13, A14, C3 to C12, E1, E2, E13, E14	JGND	Ground	Not applicable	JESD Ground.
A3, B3	SERDOUT_N[1], SERDOUT_P[1]	Output	JESD204B	Lane 1 Differential Pair.
A4, B4	SERDOUT_N[0], SERDOUT_P[0]	Output	JESD204B	Lane 0 Differential Pair.
A5, B5	SERDOUT_N[2], SERDOUT_P[2]	Output	JESD204B	Lane 2 Differential Pair.
A6, B6	SERDOUT_N[4], SERDOUT_P[4]	Output	JESD204B	Lane 4 Differential Pair.
A7, B7	SERDOUT_N[6], SERDOUT_P[6]	Output	JESD204B	Lane 6 Differential Pair.
A8, B8	SERDOUT_N[8], SERDOUT_P[8]	Output	JESD204B	Lane 8 Differential Pair.
A9, B9	SERDOUT_N[10], SERDOUT_P[10]	Output	JESD204B	Lane 10 Differential Pair.
A10, B10	SERDOUT_N[12], SERDOUT_P[12]	Output	JESD204B	Lane 12 Differential Pair.
A11, B11	SERDOUT_N[14], SERDOUT_P[14]	Output	JESD204B	Lane 14 Differential Pair.
A12, B12	SERDOUT_N[15], SERDOUT_P[15]	Output	JESD204B	Lane 15 Differential Pair.
B1, B2	SERDOUT_N[3], SERDOUT_P[3]	Output	JESD204B	Lane 3 Differential Pair.
B13, B14	SERDOUT_P[13], SERDOUT_N[13]	Output	JESD204B	Lane 13 Differential Pair.
C1, C2	SERDOUT_N[5], SERDOUT_P[5]	Output	JESD204B	Lane 5 Differential Pair.
C13, C14	SERDOUT_P[11], SERDOUT_N[11]	Output	JESD204B	Lane 11 Differential Pair.
D1, D2	SERDOUT_N[7], SERDOUT_P[7]	Output	JESD204B	Lane 7 Differential Pair.

Pin No.	Ball Mnemonic	Ball Type	Signal Type	Description
D3, E3, E10, E11, F3, J12, K12, L12, N14, P12, P13	RES_DNC	Not applicable	Not applicable	Reserved. Do not connect.
D4, D5, D10, D11	JVTT	Supply	Not applicable	JESD204B Output Driver Termination Voltage, 1 V Supply.
D6 to D9	JVDD	Supply	Not applicable	JESD204B Digital Circuitry Supply, 1 V Supply.
D12	JVDD2	Supply	Not applicable	2 V Supply for JESD204B.
D13, D14	SERDOUT_P[9], SERDOUT_N[9]	Output	JESD204B	Lane 9 Differential Pair.
E4	TIE_LOW	Input	CMOS	Internal Use Only. Connect to ground.
E5 to E9, F4 to F6, F9, F10	DGND	Ground	Not applicable	Digital Ground.
E12, F2	SVDD2	Supply	Not applicable	2 V Supply for Digital Input/Output and SPI.
F1, G1	SYNCINB_P, SYNCINB_N	Input	Not applicable	JESD204B Synchronization. When low, the JESD204B interface handshakes with the receiver. This pin goes high when handshake is complete.
F7, F8, G5 to G10	DVDD	Supply	Not applicable	1 V Supply for Digital Core.
F11, G13	AVSSFS8	Ground	Not applicable	Ground for AVSSFS8 Supply Domain. Connect to ground.
F12	SCLK	Input	Not applicable	Main SPI Clock Pin.
F13	CSB	Input	Not applicable	Chip Select Pin for SPI.
F14, G14	SYSREF_N, SYSREF_P	Input/output	LVDS/CML	Differential Synchronization Signal. Critical timing relative to CLK_x. This pin is placed near CLK_x inputs and establishes deterministic latency. This pin is internally tied to ground through 50 Ω in default configuration and can be left floating if set to Subclass 0 mode via Register 0x525.
G2	TMU_REFP	Input	Static	TMU Reference Supply. Connect this pin to a clean, 1.8 V reference supply on the board that is ≤TMU_AVDD2.
G3, H3	TDN, TDP		Static	Temperature Diode Cathode/Anode. This pin can be left floating if unused.
G4	TMU_DVDD1	Supply	Not applicable	Temperature Measurement Unit (TMU) Digital Domain Supply.
G11	AVDDFS8	Supply	Not applicable	1 V Supply for Clocks with f_S/8 Energy.
G12	SDIO	Input/output	Not applicable	Main SPI Input/Output Pin.
H1	FD	Output	CMOS	Fast Detect Pin.
H2	TMU_REFN	Input	Static	TMU Reference Supply. Connect to clean ground on board.
H4, H11	VSS_MOAT	Ground	Not applicable	Ground for Isolation Guard Ring. Connect to ground.
H5 to H10, J14, K2 to K11, L6 to L11, M6, M9, M13, M14, N4, N6, N9, N12, N13, P1, P6, P9, P11, P14	AGND	Ground	Not applicable	Ground for ADC.
H12, J3 to J11, J13	AVDD	Supply		Analog Core 1 V Supply for ADC.
H13, H14	TRIG_P, TRIG_N	Input	LVDS	Trigger Input for Frequency Hopping. This pin is internally tied to ground through 50 Ω in default configuration and can be left floating if disabled by default with Register 0x602.
J1, J2	VDD_NVG	Supply		1 V supply for onboard Negative Voltage Generator (NVG).
K1	VNEG_OUT	Output		Internally Generated −1 V Output.
K13, L13	CLKVDD_LF	Supply		1 V Supply for Clock Buffer.
K14, L14	CLK_N, CLK_P	Input	RF	Clock Inputs, High Frequency.
L1, L2	VSS_NVG	Ground		Supply Voltage (VSS) for NVG.
L3	TMU_AVDD2	Supply		TMU 2 V Analog Supply.
L4	RVDD2	Supply		TOP_REF 2 V Supply.

Pin No.	Ball Mnemonic	Ball Type	Signal Type	Description
L5	BVDD3	Supply		Internally Generated 3 V Supply for Input Buffer. Bypass with 10 μF and 0.1 μF capacitors to GND.
M1, M2, M3, N2, P2	GPIO[4], GPIO[2], GPIO[3], GPIO[1], GPIO[0]	Input/output		General-Purpose Input/Output Pins. These pins can be left floating in default configuration.
M4	BVNN2	Supply	Not applicable	Internally Generated −2 V Supply for Input Buffer. Bypass with 10 μF and 0.1 μF capacitors to GND.
M5, N5, P5	BVNN1	Supply	Not applicable	−1 V Supply for Input Buffer.
M7, M8, N7, N8	VOID	Not applicable	Not applicable	No Balls at These Locations.
M10, N10, P10	BVDD2	Supply	Not applicable	2 V supply for Input Buffer.
M11	FVDD	Supply	Not applicable	1 V Supply for Reference ADC (REF_ADC).
M12	PLLVDD2	Supply	Not applicable	2.0 V LDO Supply.
N1	RSTB	Input	Not applicable	Chip Reset, Active Low.
N3	VREF	Input	Static	Optional VREF Import.
N11	PDWN	Input	CMOS	Powerdown/Standby Mode Control.
P3	VCM	Output	Static	Export VCM.
P4	AVNN1	Supply	Not applicable	−1 V Supply for TOP_REF.
P7, P8	VIN_P, VIN_N	Input	RF	ADC Inputs, High Frequency.

TYPICAL PERFORMANCE CHARACTERISTICS

AD9213-6G

Nominal supply voltages, sampling rate = 6 GSPS, 1.4 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, T_J = 70°C, 128k FFT, unless otherwise noted.

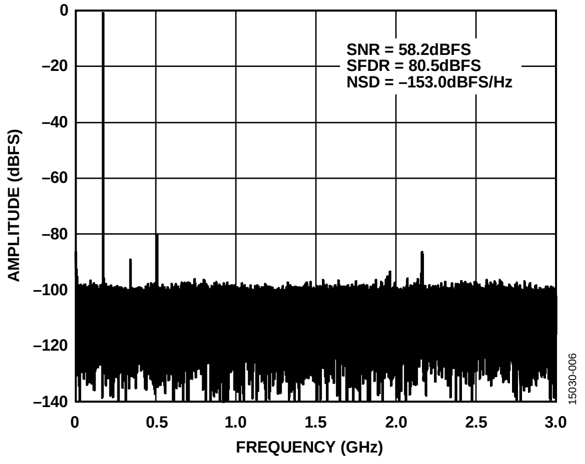


Figure 6. Single-Tone FFT with f_{IN} = 170 MHz, 6 GSPS

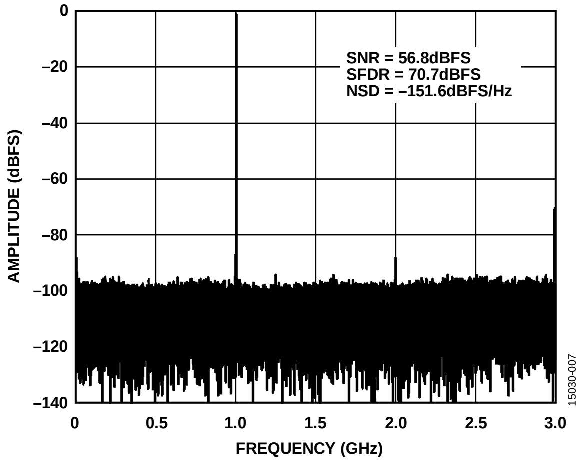


Figure 7. Single-Tone FFT with f_{IN} = 1 GHz, 6 GSPS

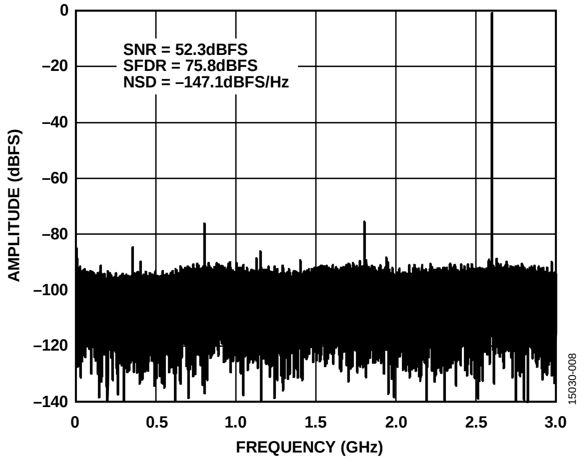


Figure 8. Single-Tone FFT with f_{IN} = 2.6 GHz, 6 GSPS

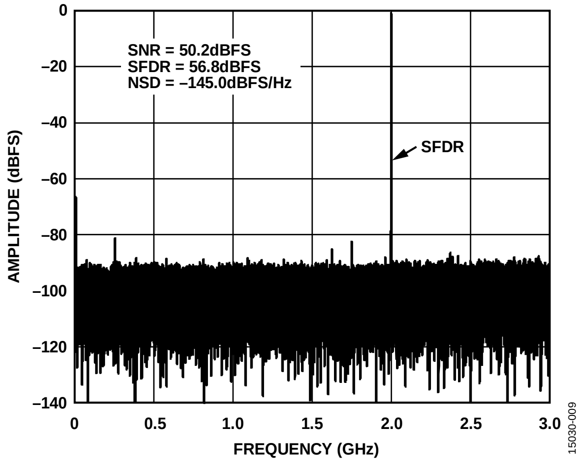


Figure 9. Single-Tone FFT with f_{IN} = 4 GHz, 6 GSPS

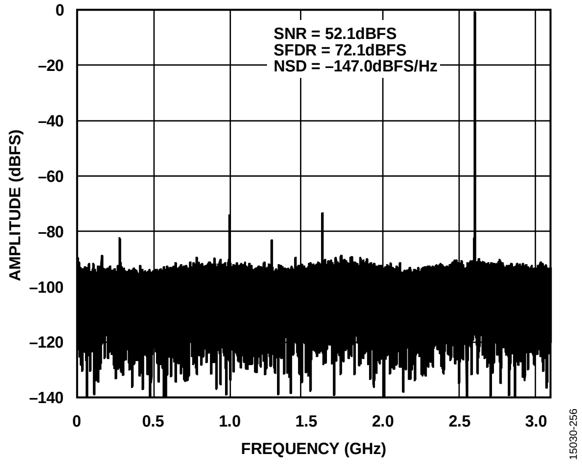


Figure 10. Single Tone FFT with f_{IN} = 2.6 GHz, Sampling Frequency = 6.2 GSPS

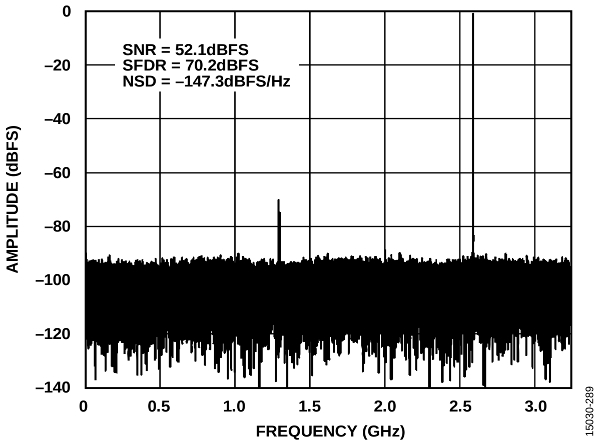


Figure 11. Single Tone FFT with f_{IN} = 2.6 GHz, Sampling Frequency = 6.5 GSPS

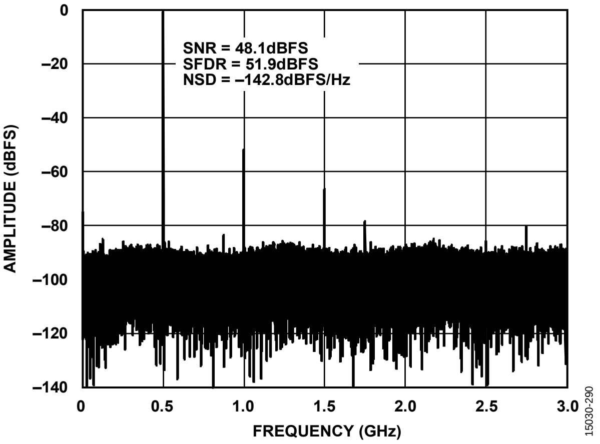


Figure 12. Single-Tone FFT with f_{IN} = 5.5 GHz, 6 GSPS

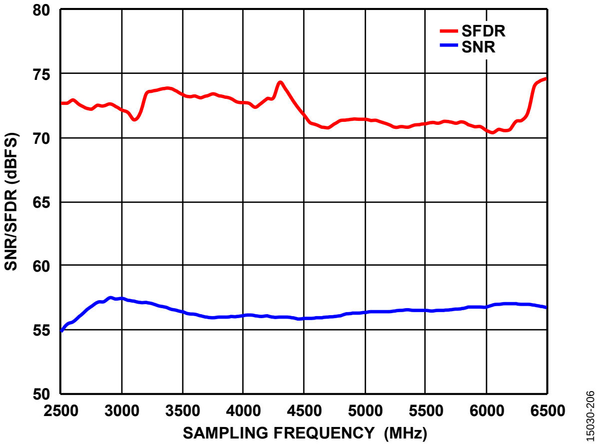


Figure 15. SNR/SFDR vs. Sampling Frequency, f_{IN} = 1000 MHz, 6 GSPS

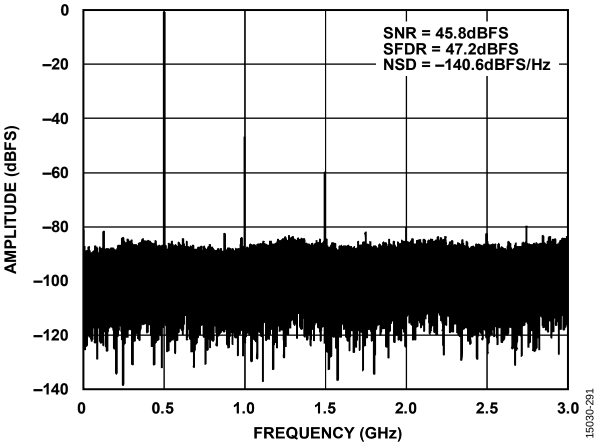


Figure 13. Single-Tone FFT with f_{IN} = 6.5 GHz, 6 GSPS

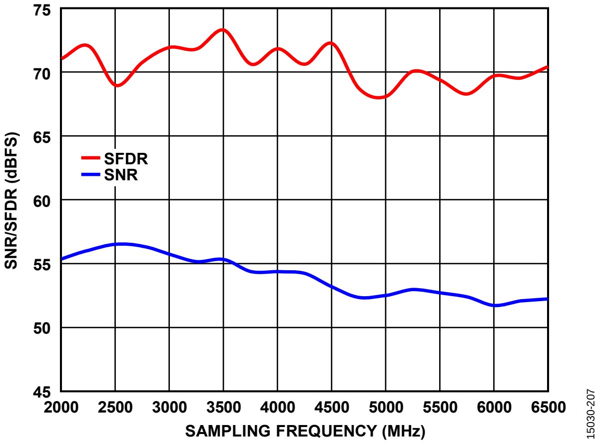


Figure 16. SNR/SFDR vs. Sampling Frequency, f_{IN} = 2.6 GHz, 6 GSPS

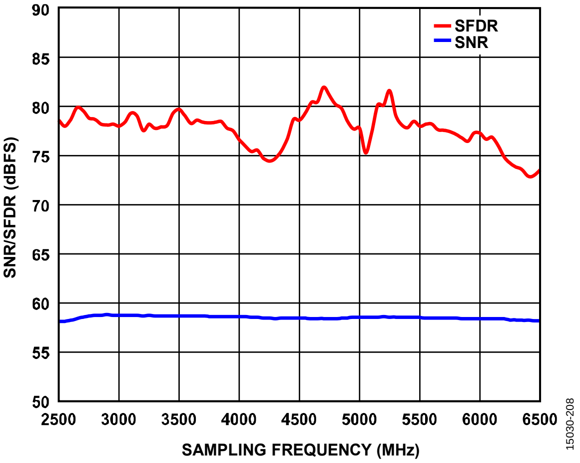


Figure 14. SNR/SFDR vs. Sampling Frequency, f_{IN} = 170 MHz, 6 GSPS

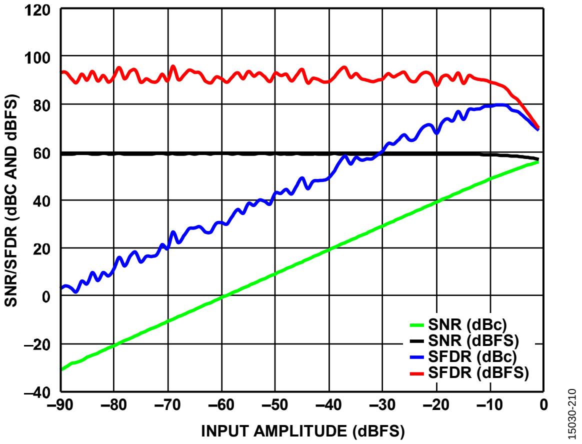


Figure 17. SNR/SFDR vs. Input Amplitude, f_{IN} = 1000 MHz, 6 GSPS

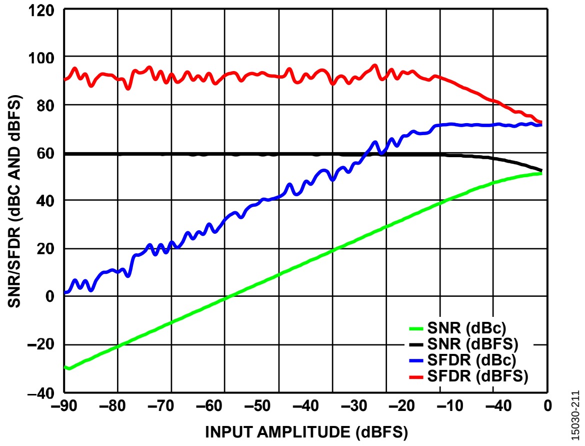


Figure 18. SNR/SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 2600 MHz, 6 GSPS

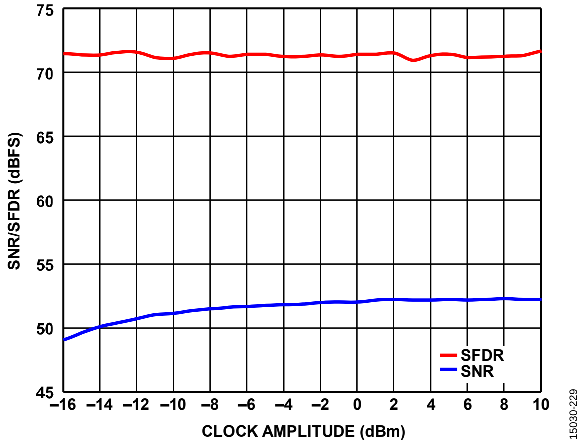


Figure 21. SNR/SFDR vs. Clock Amplitude at f_{IN} = 2600 MHz, 6 GSPS

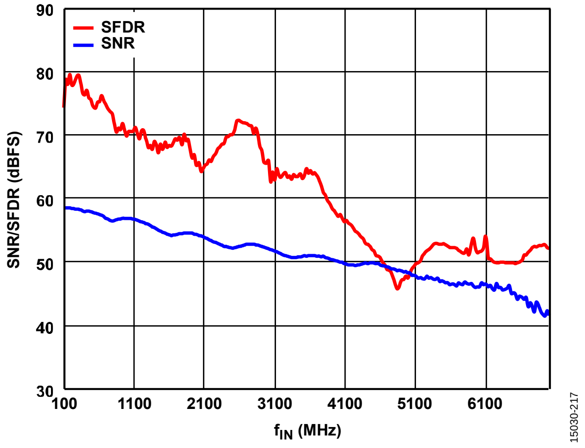


Figure 19. SNR/SFDR vs. f_{IN}, A_{IN} = –1 dBFS, 6 GSPS

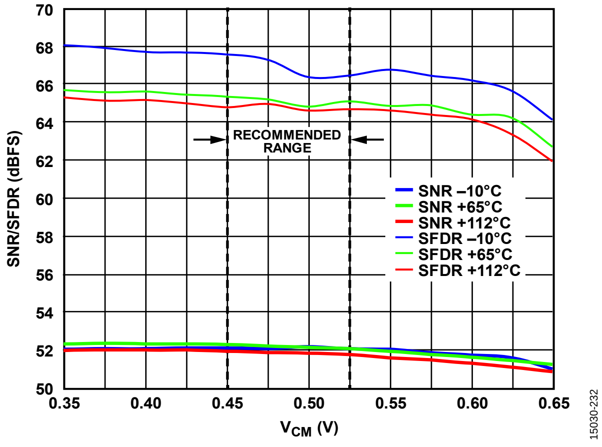


Figure 22. SNR/SFDR vs. V_{CM}, f_{IN} = 2600 MHz, 6 GSPS, Temperatures Shown = T_J

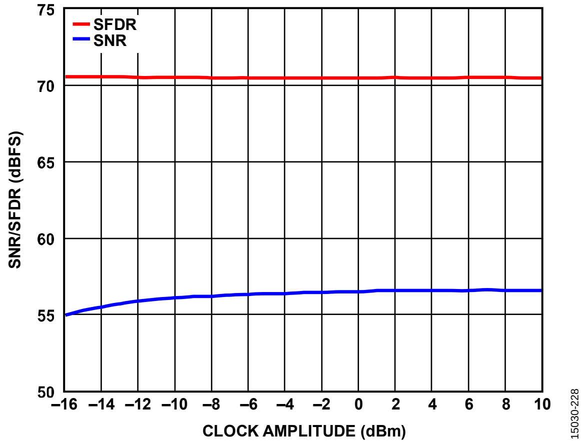


Figure 20. SNR/SFDR vs. Clock Amplitude at f_{IN} =1000 MHz, 6 GSPS

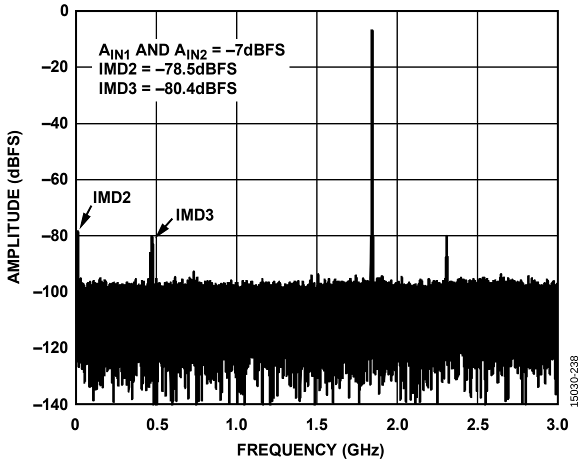


Figure 23. Two-Tone FFT, f_{IN1} = 1841.5 MHz, f_{IN2} = 1846.5 MHz, A_{IN1} and A_{IN2} = –7 dBFS, 6 GSPS

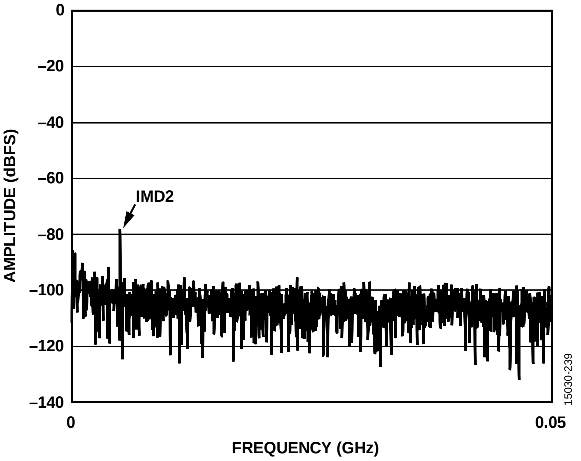


Figure 24. Two-Tone FFT, IMD2 Zoom In, f_{IN1} = 1841.5 MHz, f_{IN2} = 1846.5 MHz, A_{IN1} and A_{IN2} = −7 dBFS (see Figure 23), 6 GSPS

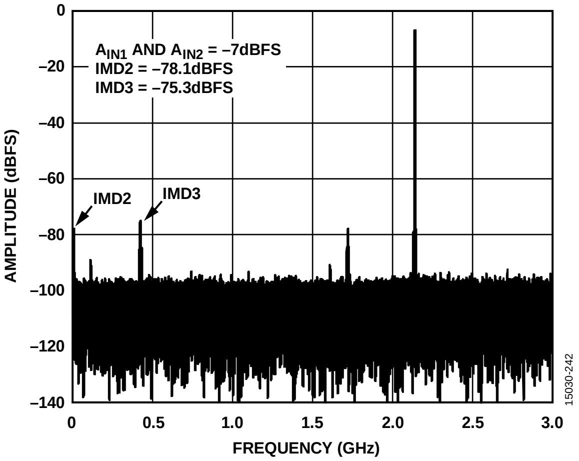


Figure 27. Two-Tone FFT, f_{IN1} = 2137.5 MHz, f_{IN2} = 2142.5 MHz, A_{IN1} and A_{IN2} = −7 dBFS, 6 GSPS

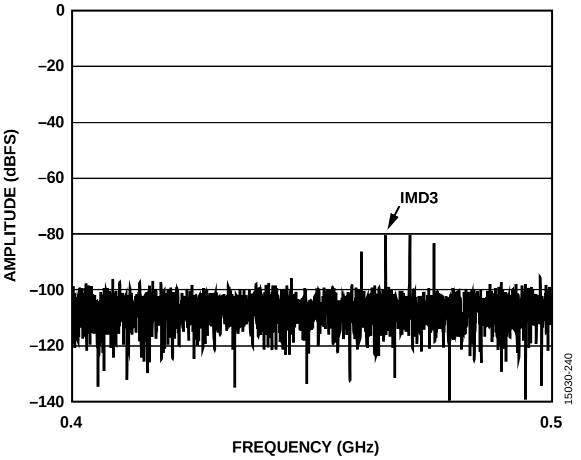


Figure 25. Two-Tone FFT, IMD3 Zoom In, f_{IN1} = 1841.5 MHz, f_{IN2} = 1846.5 MHz, A_{IN1} and A_{IN2} = −7 dBFS (see Figure 23), 6 GSPS

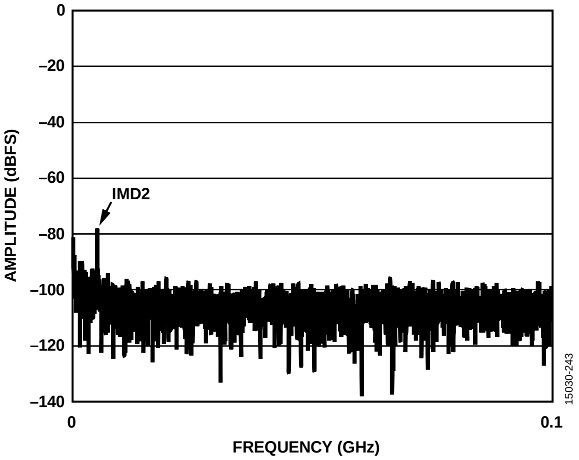


Figure 28. Two-Tone FFT, IMD2 Zoom In, f_{IN1} = 2137.5 MHz, f_{IN2} = 2142.5 MHz, A_{IN1} and A_{IN2} = −7 dBFS, 6 GSPS

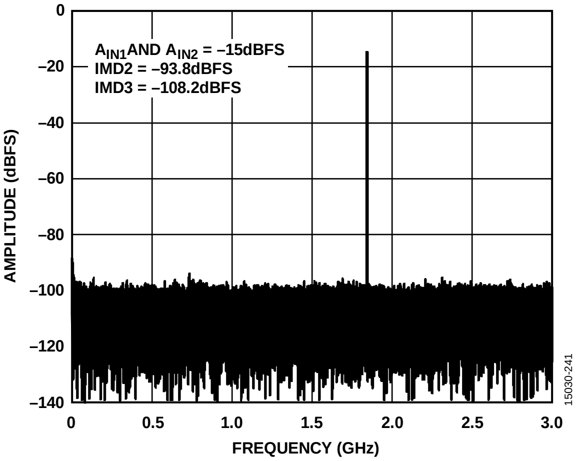


Figure 26. Two-Tone FFT, f_{IN1} = 1841.5 MHz, f_{IN2} = 1846.5 MHz, A_{IN1} and A_{IN2} = −15 dBFS, 6 GSPS

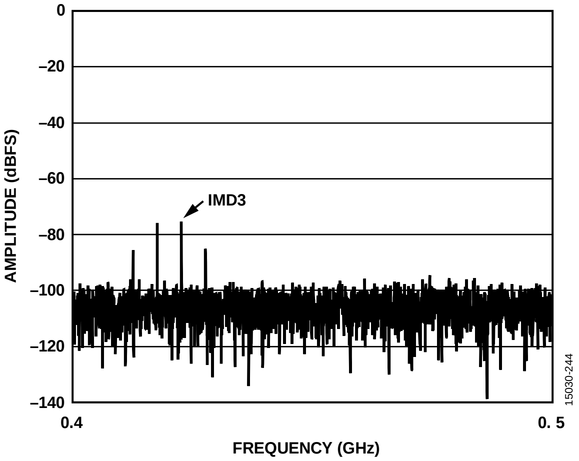


Figure 29. Two-Tone FFT, IMD3 Zoom In, f_{IN1} = 2137.5 MHz, f_{IN2} = 2142.5 MHz, A_{IN1} and A_{IN2} = −7 dBFS, 6 GSPS

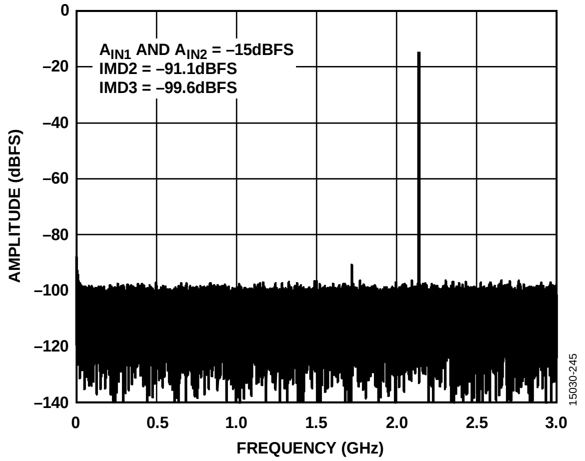


Figure 30. Two-Tone FFT, f_{IN1} = 2137.5 MHz, f_{IN2} = 2142.5 MHz, A_{IN1} and A_{IN2} = −15 dBFS, 6 GSPS

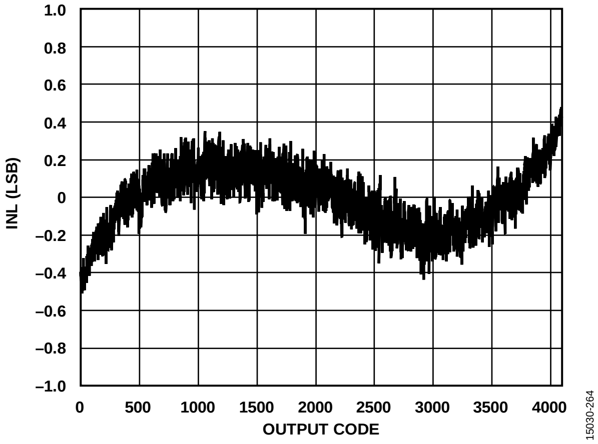


Figure 31. INL at f_{IN} =170 MHz, 6 GSPS

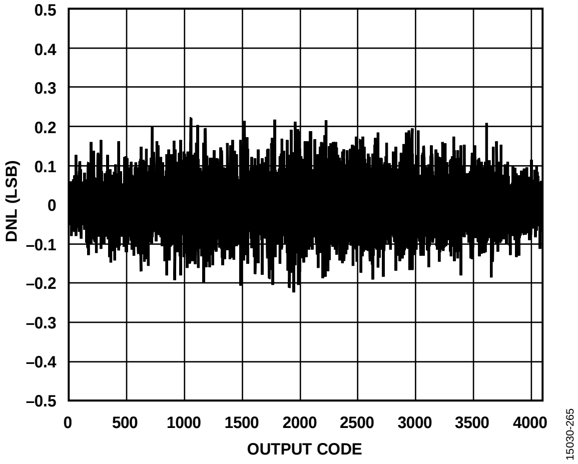


Figure 32. DNL at f_{IN} =170 MHz, 6 GSPS

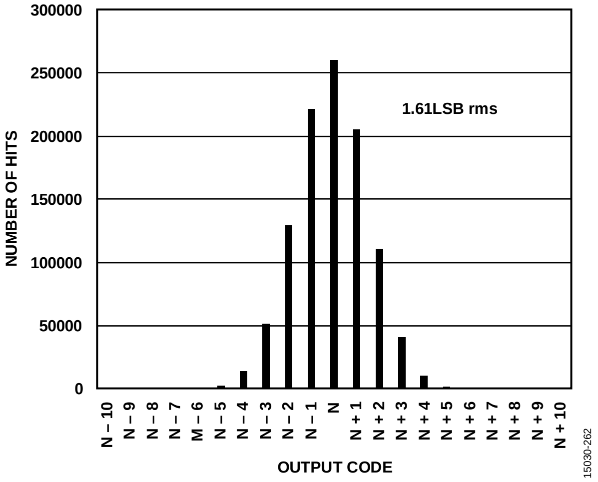


Figure 33. Input Referred Noise Histogram, 6 GSPS

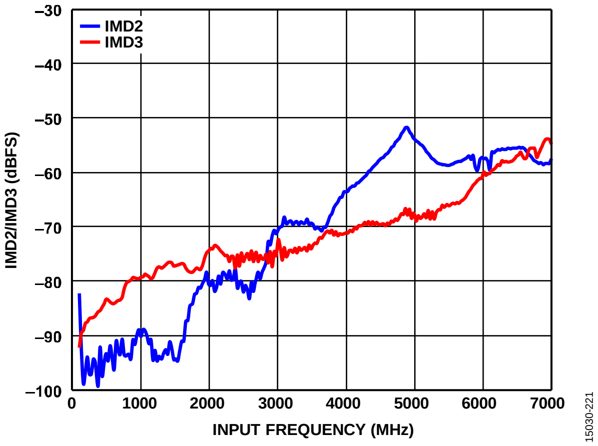


Figure 34. IMD2/IMD3 vs. Input Frequency (A_{IN} = −7dBFS), 10 MHz Spacing, 6 GSPS

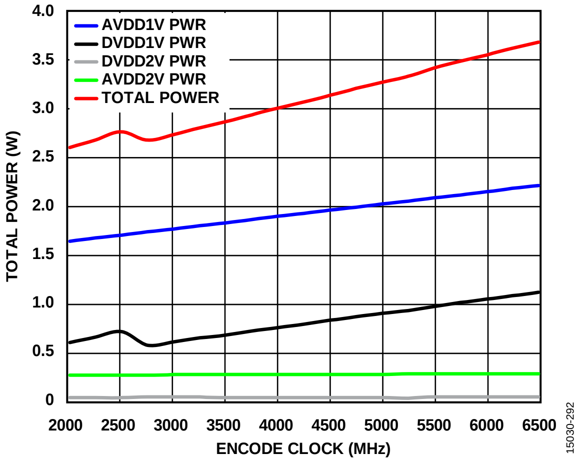


Figure 35. Total Power vs. Encode Clock (f_S) For 16 SERDES Lanes, f_{IN} = 2600 MHz

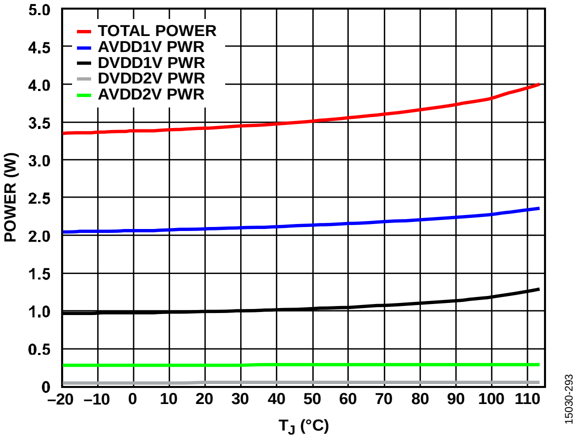


Figure 36. Power vs. Junction Temp (T_J), f_{IN} = 2600 MHz, 6 GSPS

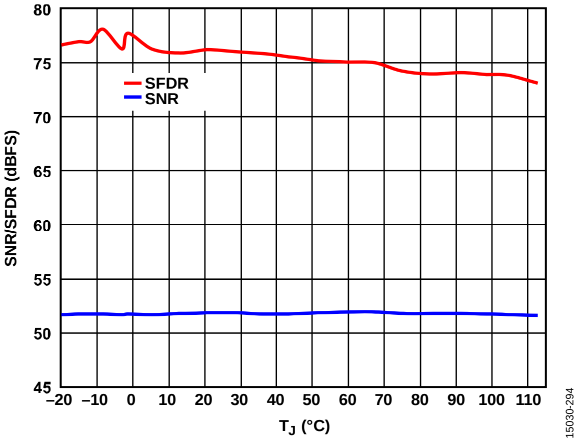


Figure 37. SNR/SFDR vs. T_J, f_{IN} = 2600 MHz, 6 GSPS

AD9213-10G

Nominal supply voltages, sampling rate = 10 GSPS, 1.4 V p-p full-scale differential input, A_{IN}= −1.0 dBFS, T_J = 70°C, 128k FFT, unless otherwise noted.

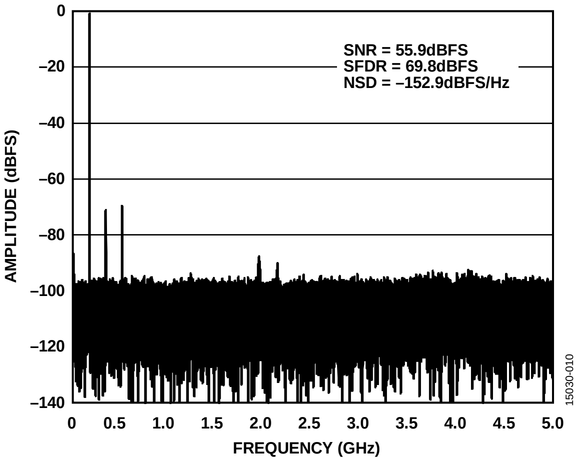


Figure 38. Single-Tone FFT with f_{IN} = 170 MHz, 10 GSPS

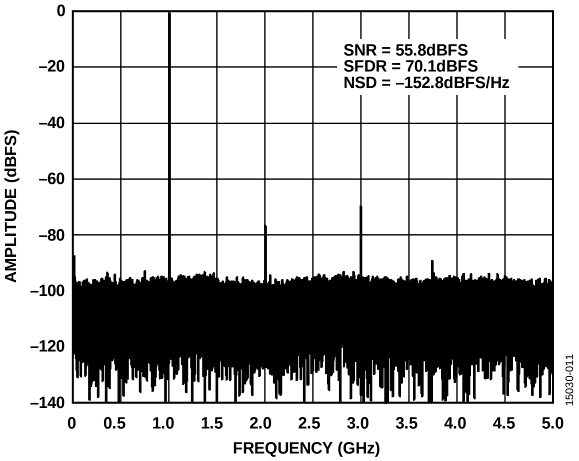


Figure 39. Single-Tone FFT with f_{IN} = 1 GHz, 10 GSPS

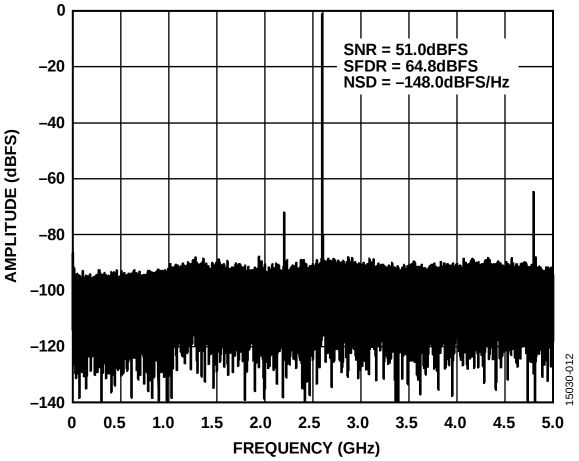


Figure 40. Single-Tone FFT with f_{IN} = 2.6 GHz, 10 GSPS

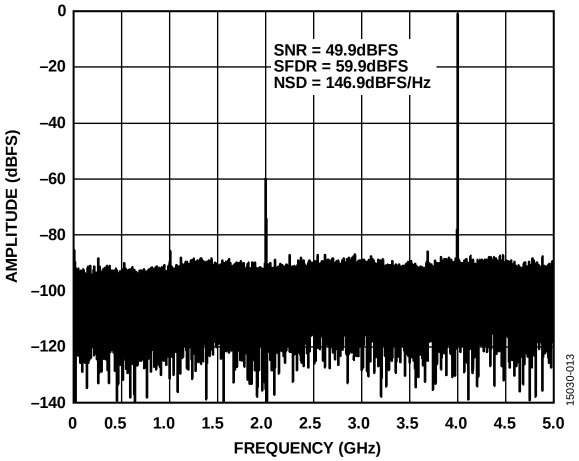


Figure 41. Single-Tone FFT with f_{IN} = 4 GHz, 10 GSPS

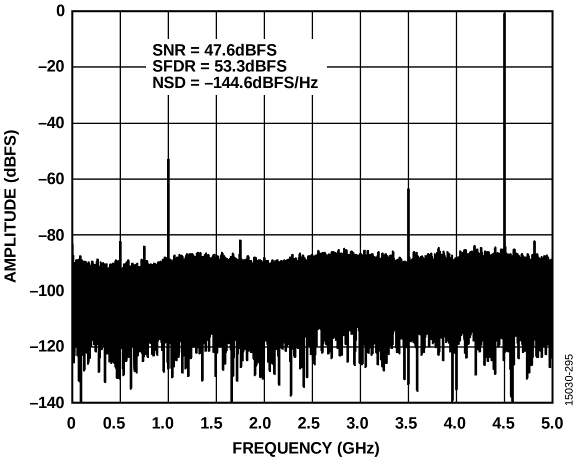


Figure 42. Single-Tone FFT with f_{IN} = 5.5 GHz, 10 GSPS

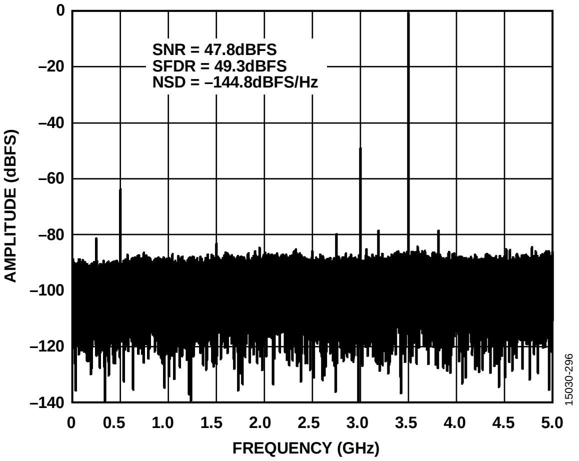


Figure 43. Single-Tone FFT with f_{IN} = 6.5 GHz, 10 GSPS

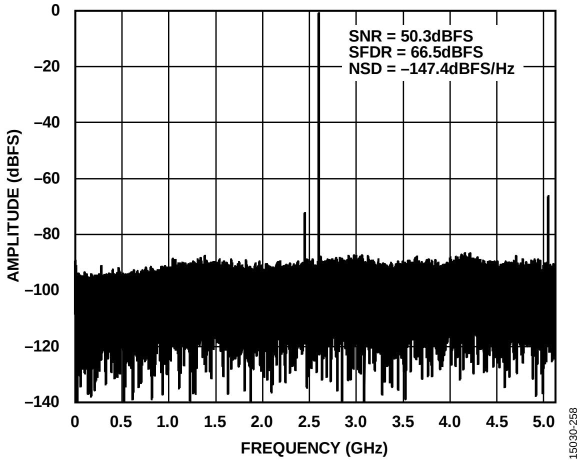


Figure 44. Single-Tone FFT with f_{IN} = 2.6 GHz, 10.25 GSPS

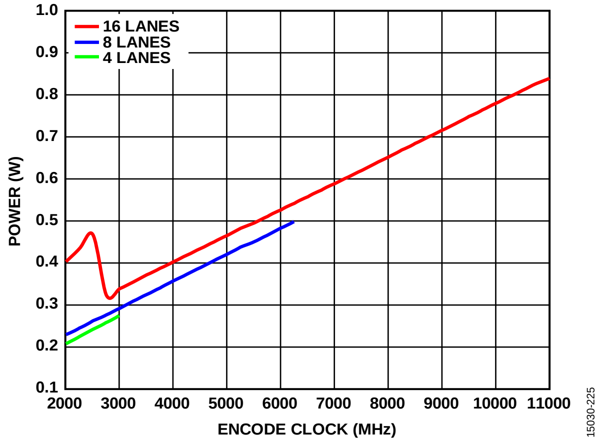


Figure 47. Power vs. Encode Clock (f_S) for a Various Number of JESD204B Lanes, f_{IN} = 170 MHz, 10 GSPS

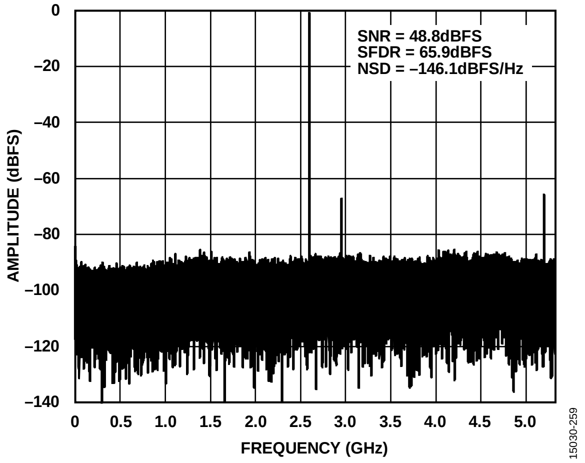


Figure 45. Single Tone FFT with f_{IN} = 2.6 GHz, 10.75 GSPS

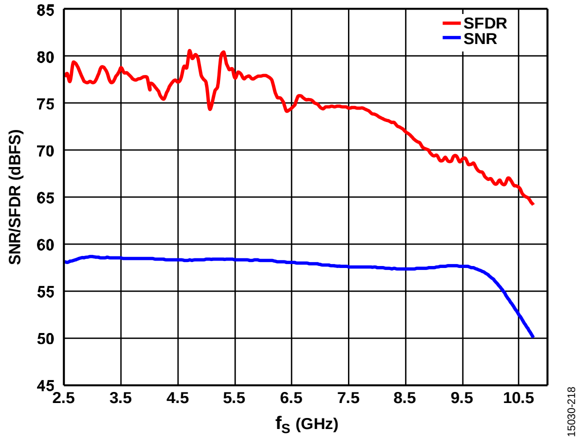


Figure 48. SNR/SFDR vs. Sampling Frequency, f_{IN} = 170 MHz

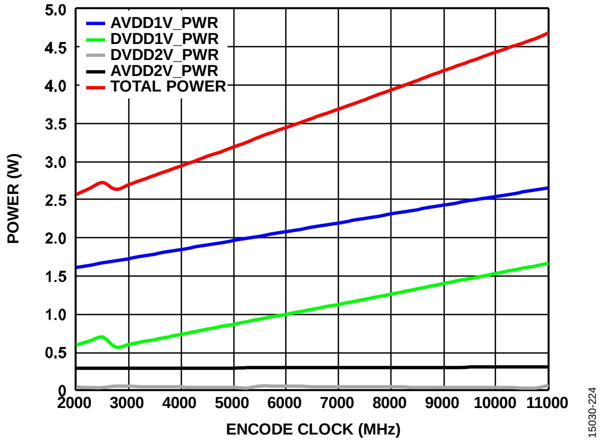


Figure 46. Power vs. Encode Clock (f_S) for 16 JESD204B Lanes, f_{IN} = 170 MHz, 10 GSPS

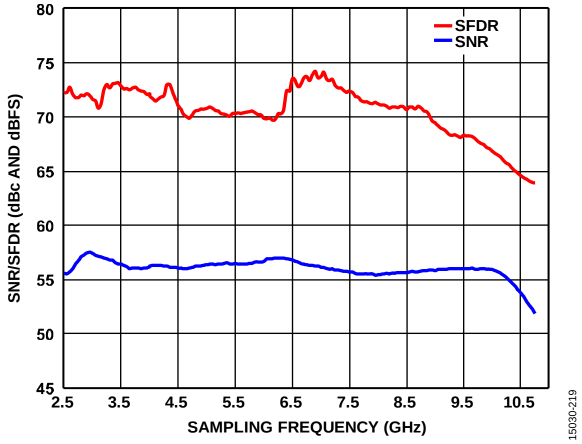


Figure 49. SNR/SFDR vs. Sampling Frequency (f_S), f_{IN} = 1000 MHz, 10 GSPS

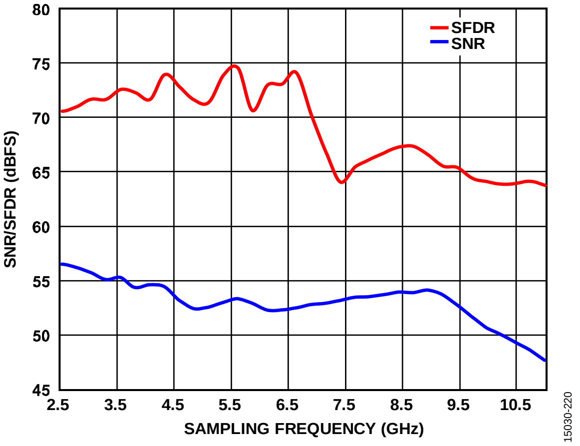


Figure 50. SNR/SFDR vs. Sampling Frequency, f_{IN} = 2600 MHz, 10 GSPS

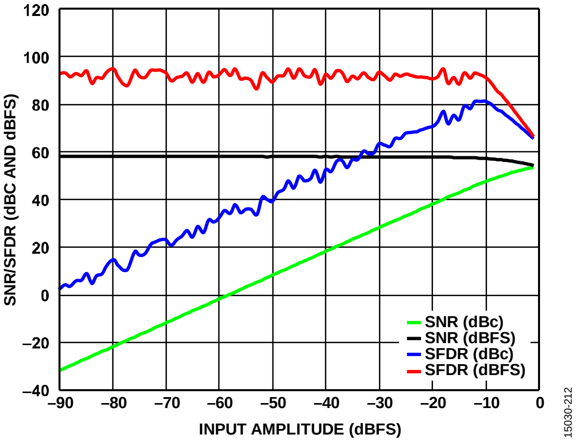


Figure 51. SNR/SFDR vs. Input Amplitude, f_{IN} = 1000 MHz, 10 GSPS

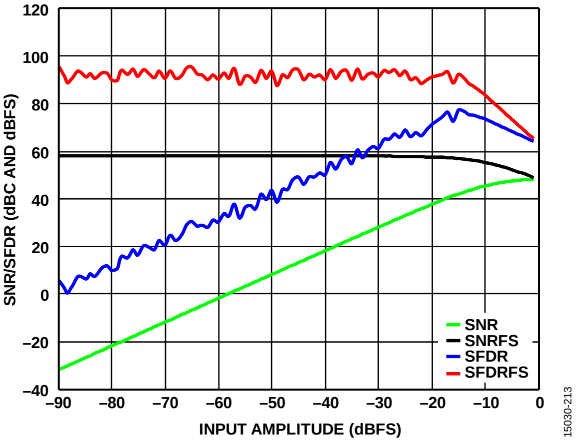


Figure 52. SNR/SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 2600 MHz, 10 GSPS

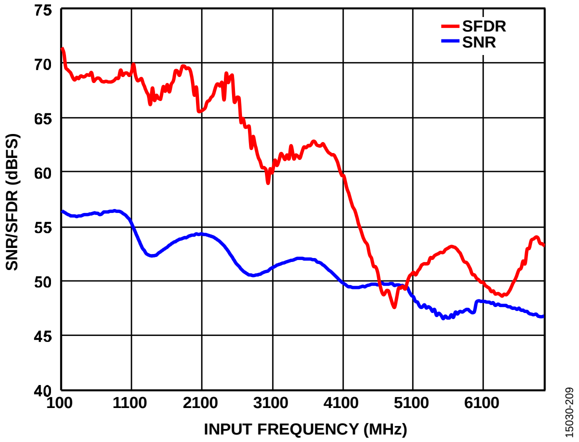


Figure 53. SNR/SFDR vs. Input Frequency (f_{IN}), 10 GSPS, A_{IN} = −1 dBFS

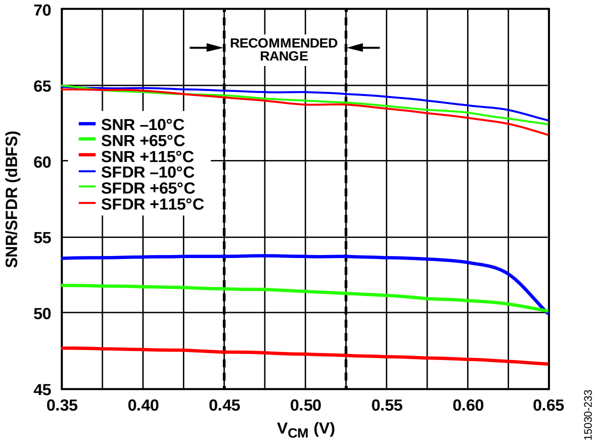


Figure 54. SNR/SFDR vs. V_{CM}, f_{IN} = 2600 MHz, 10 GSPS, Temperatures Shown = T_J

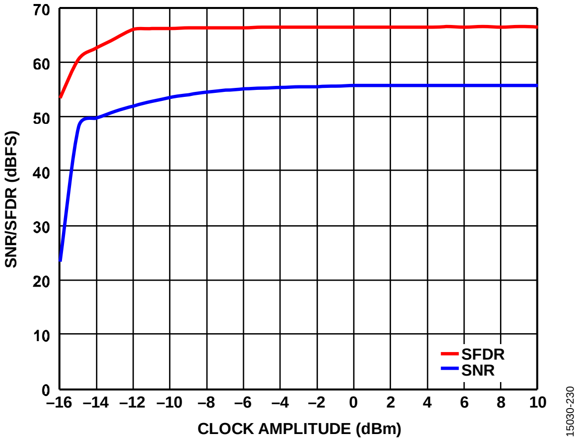


Figure 55. SNR/SFDR vs. Clock Amplitude, f_{IN} = 1000 MHz, 10 GSPS

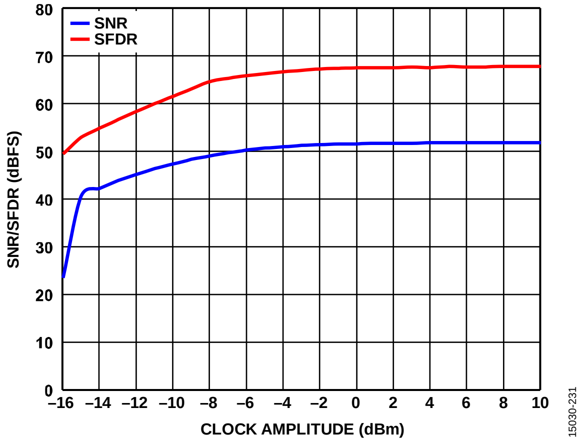


Figure 56. SNR/SFDR vs. Clock Amplitude, f_{IN} = 2600 MHz, 10 GSPS

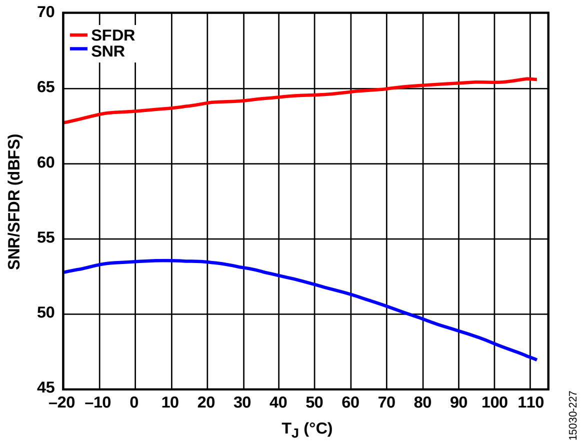


Figure 57. SNR/SFDR vs. T_J, f_{IN} = 2600 MHz, 10 GSPS

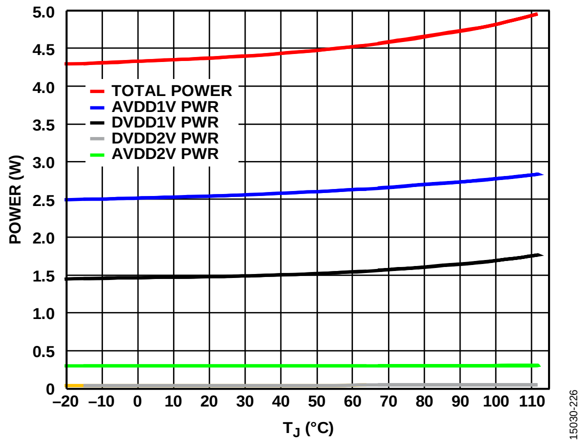


Figure 58. Power vs. T_J, f_{IN} = 2600 MHz, 10 GSPS

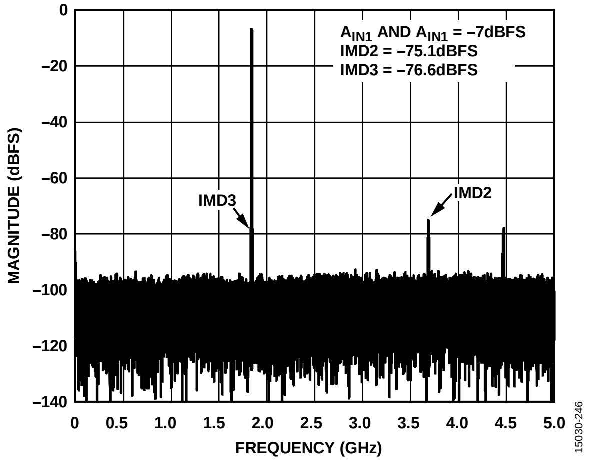


Figure 59. Two-Tone FFT, 10 GSPS, f_{IN1} = 1841.5 MHz, f_{IN2} = 1846.5 MHz, A_{IN1} and A_{IN2} = −7 dBFS

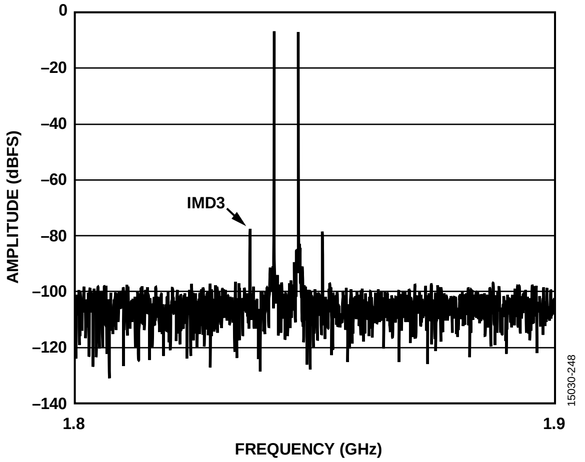


Figure 60. Two-Tone FFT, IMD3 Zoom In, f_{IN1} = 1841.5 MHz, f_{IN2} = 1846.5 MHz, A_{IN1} and A_{IN2} = −7 dBFS (see Figure 59), 10 GSPS

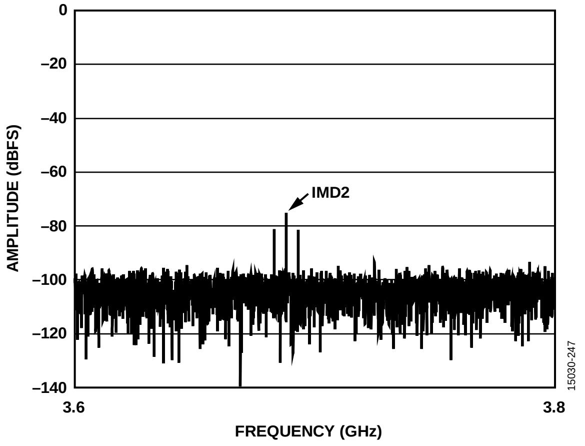


Figure 61. Two-Tone FFT, IMD2 Zoom In, f_{IN1} = 1841.5 MHz, f_{IN2} = 1846.5 MHz, A_{IN1} and A_{IN2} = −7 dBFS (see Figure 59), 10 GSPS

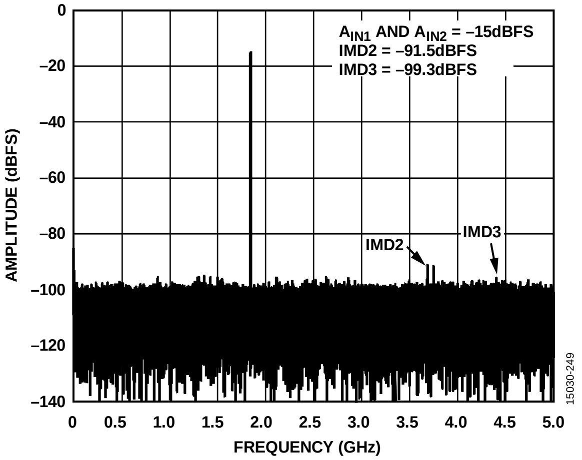


Figure 62. Two-Tone FFT, f_{IN1} = 1841.5 MHz, f_{IN2} = 1846.5 MHz, A_{IN1} and A_{IN2} = −15 dBFS, 10 GSPS

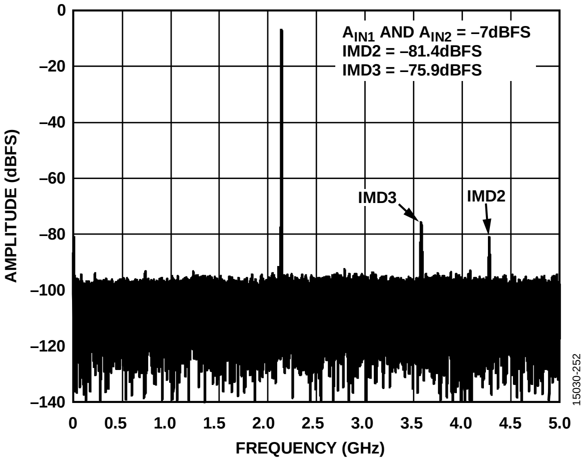


Figure 65. Two-Tone FFT, f_{IN1} = 2137.5 MHz, f_{IN2} = 2142.5 MHz, A_{IN1} and A_{IN2} = −7 dBFS, 10 GSPS

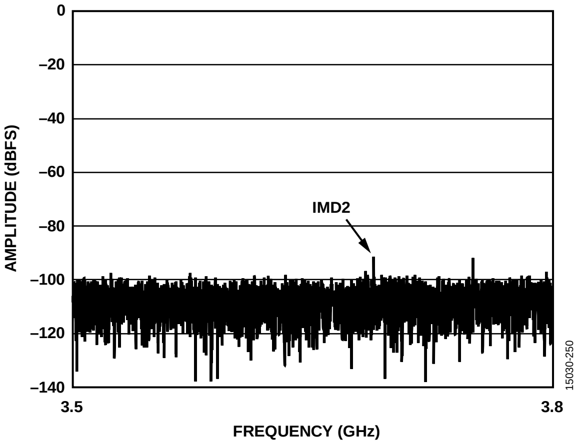


Figure 63. Two-Tone FFT, IMD2 Zoom In, f_{IN1} = 1841.5 MHz, f_{IN2} = 1846.5 MHz, A_{IN1} and A_{IN2} = −15 dBFS (see Figure 62), 10 GSPS

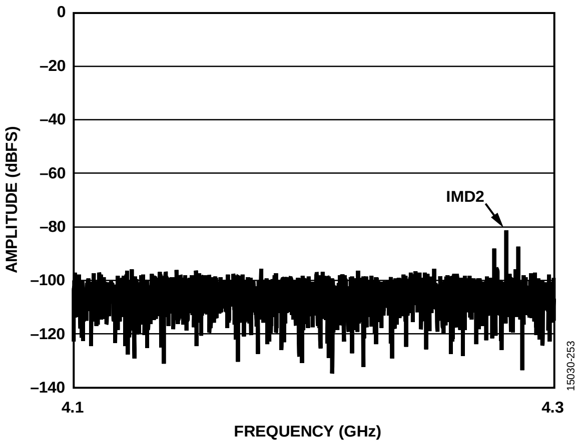


Figure 66. Two-Tone FFT, IMD2 Zoom In, f_{IN1} = 2137.5 MHz, f_{IN2} = 2142.5 MHz, A_{IN1} and A_{IN2} = −7 dBFS (see Figure 65), 10 GSPS

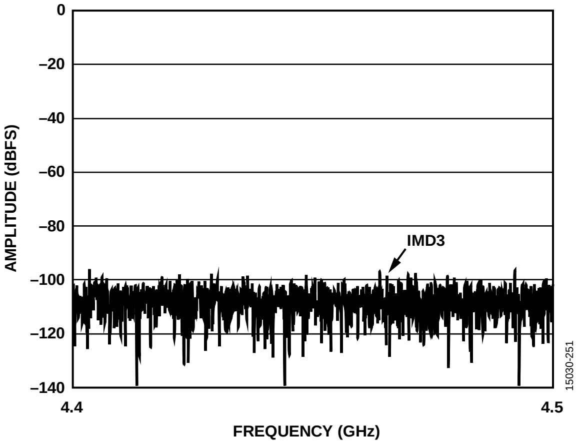


Figure 64. Two-Tone FFT, IMD3 Zoom In, f_{IN1} = 1841.5 MHz, f_{IN2} = 1846.5 MHz, A_{IN1} and A_{IN2} = −15 dBFS (see Figure 62), 10 GSPS

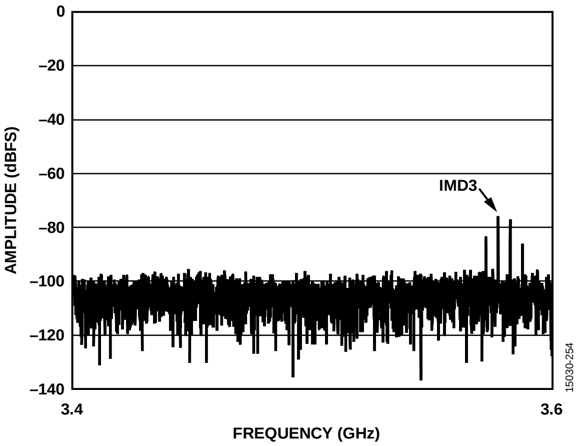


Figure 67. Two-Tone FFT, IMD3 Zoom In, f_{IN1} = 2137.5 MHz, f_{IN2} = 2142.5 MHz, A_{IN1} and A_{IN2} = −7 dBFS (see Figure 65), 10 GSPS

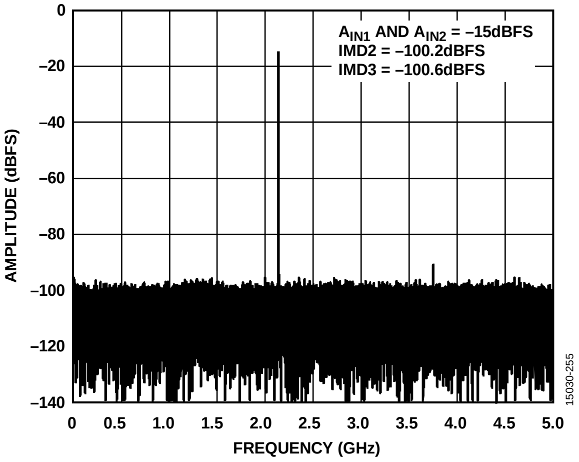


Figure 68. Two-Tone FFT, f_{IN1} = 2137.5 MHz, f_{IN2} = 2142.5 MHz, A_{IN1} and A_{IN2} = −15 dBFS, 10 GSPS

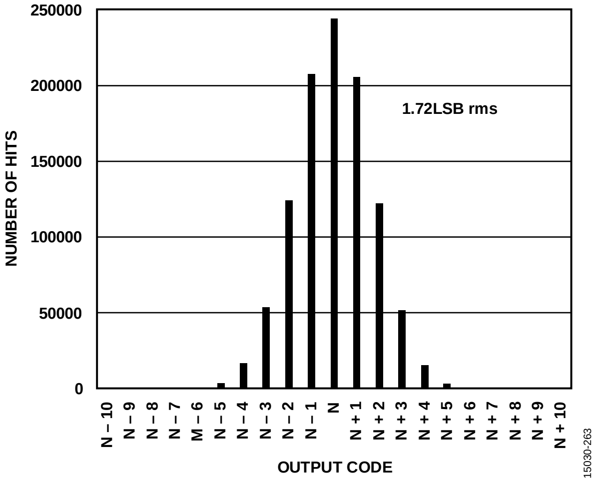


Figure 71. Input-Referred Noise Histogram, 10 GSPS

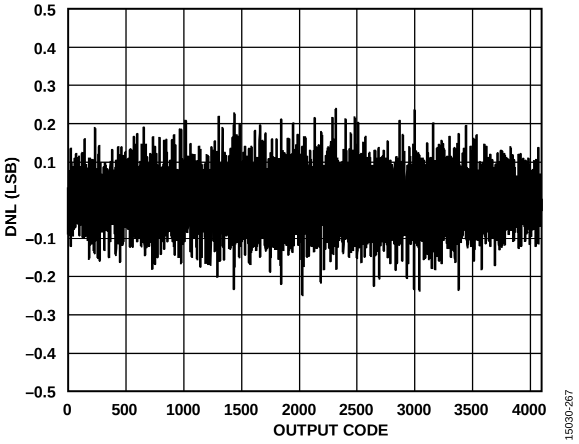


Figure 69. DNL at f_{IN} = 170 MHz, 10 GSPS

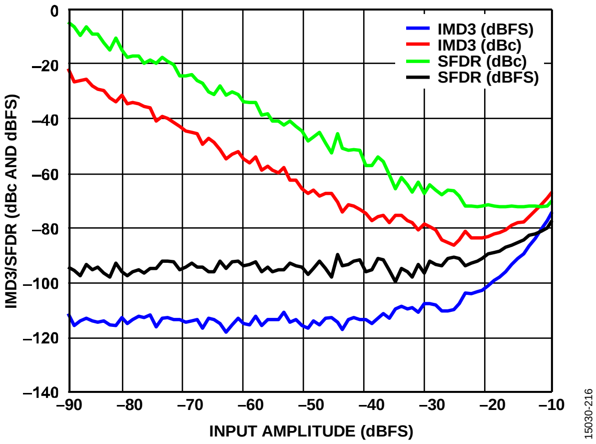


Figure 72. IMD3/SFDR vs. Input Amplitude, f_{IN1} = 2137.5 MHz, f_{IN2} = 2142.5 MHz, 10 GSPS

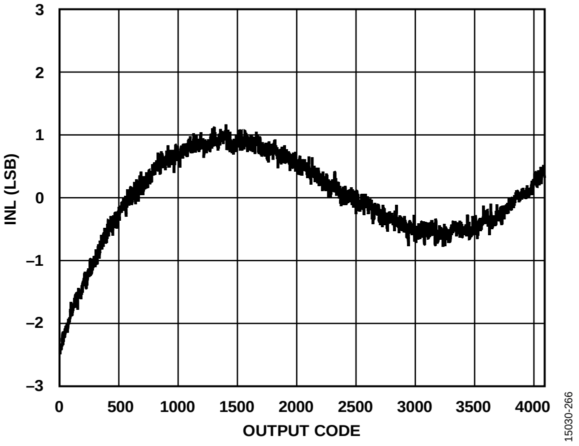


Figure 70. INL at f_{IN} = 170 MHz, 10 GSPS

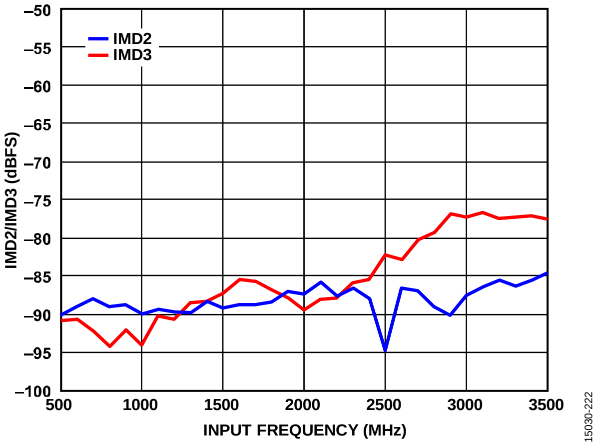


Figure 73. IMD2/IMD3 vs. Input Frequency, (A_{IN} = −7 dBFS), 100 MHz Spacing, 10 GSPS

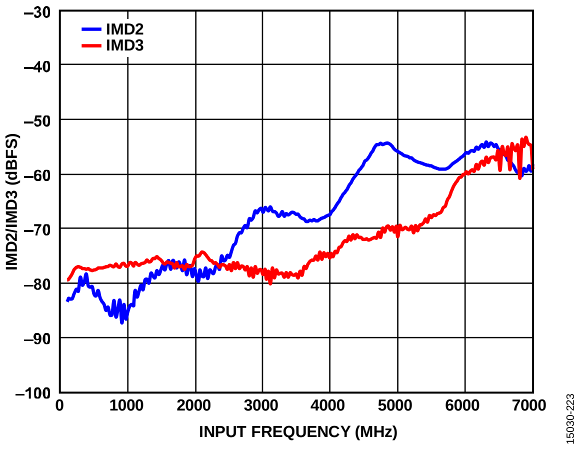


Figure 74. IMD2/IMD3 vs. Input Frequency (A_{IN} = −7 dBFS), 10 MHz Spacing, 10 GSPS

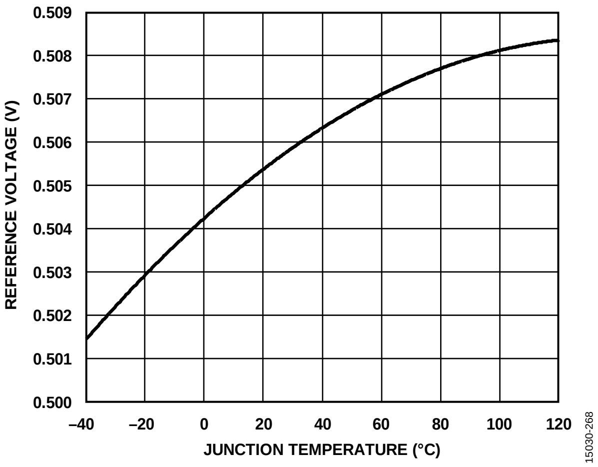


Figure 75. Reference Voltage vs. Junction Temperature, 10 GSPS

EQUIVALENT CIRCUITS

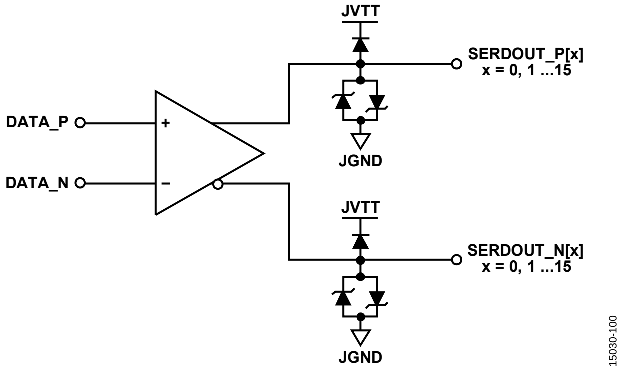


Figure 76. Digital Outputs

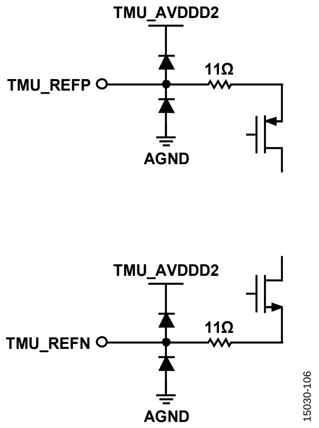


Figure 79. TMU_REFx Inputs

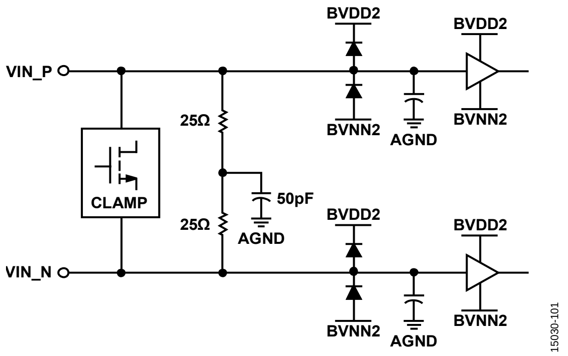


Figure 77. Analog Inputs

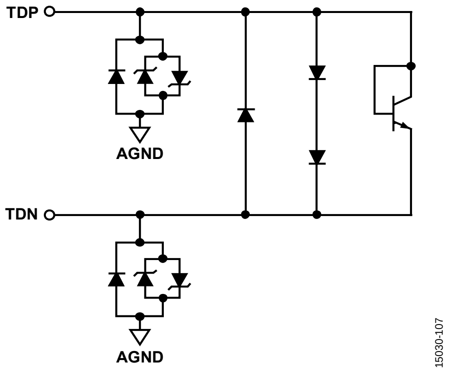


Figure 80. TDx Temperature Diodes

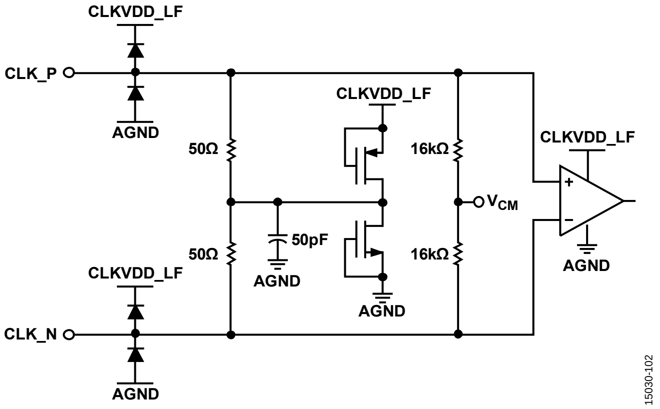
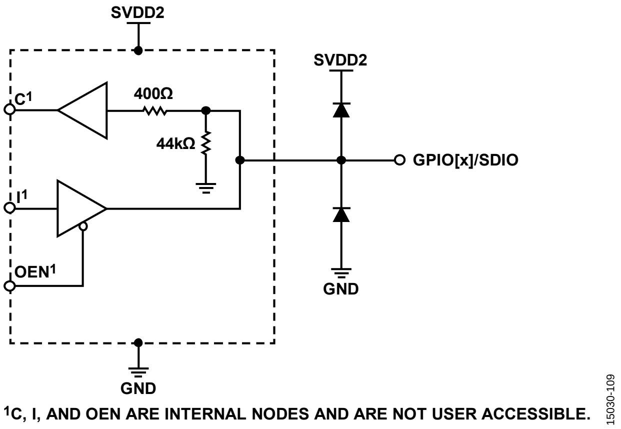


Figure 78. Clock Inputs



[1] C, I, AND OEN ARE INTERNAL NODES AND ARE NOT USER ACCESSIBLE.

Figure 81. GPIO[x] and SDIO

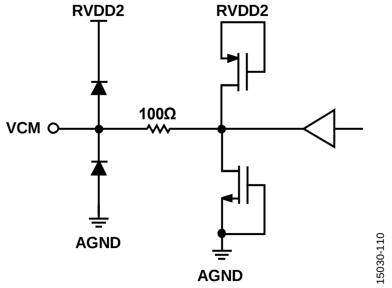
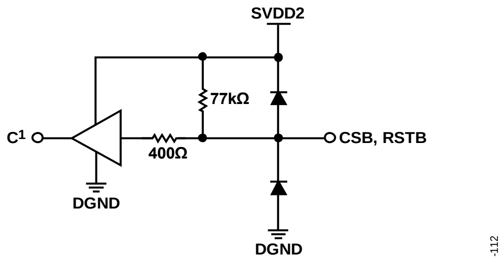


Figure 82. VCM



[1] C IS AN INTERNAL NODE AND IS NOT USER ACCESSIBLE.

Figure 83. CSB and RSTB

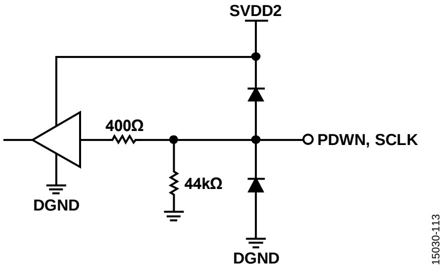
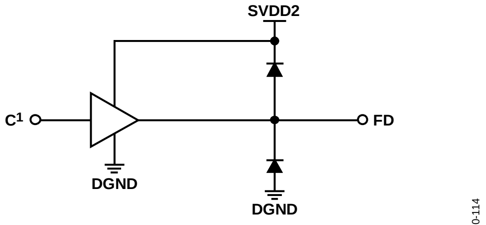


Figure 84. PDWN and SCLK



[1] C IS AN INTERNAL NODE AND IS NOT USER ACCESSIBLE.

Figure 85. FD

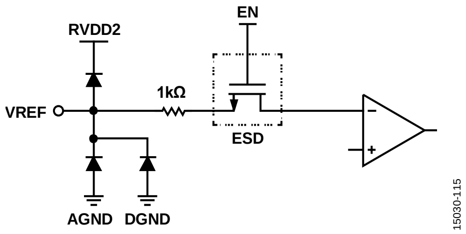


Figure 86. VREF

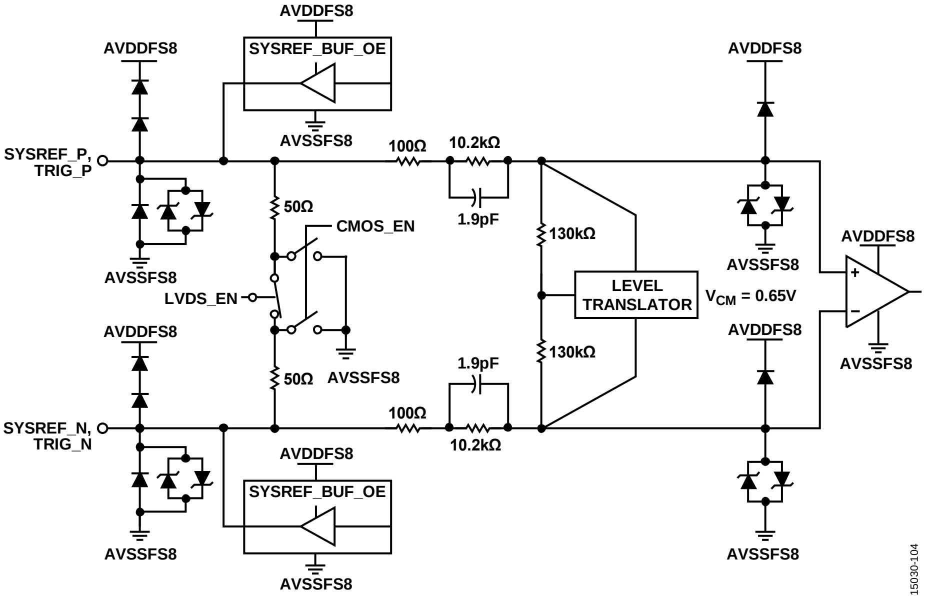


Figure 87. SYSREF_x and TRIG_x Inputs

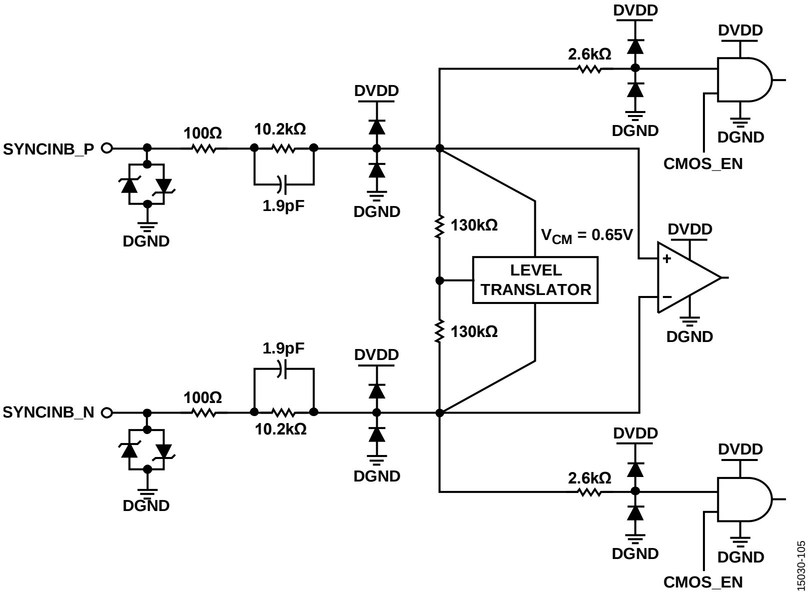


Figure 88. SYNCINB_x Inputs

THEORY OF OPERATION

The AD9213 is a single ADC with 16 JESD204B output lane pairs. The ADC is designed to sample wide bandwidth analog signals of up to 6.5 GHz. The AD9213 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. The AD9213 analog input features wide input bandwidth that supports a variety of input ranges. An integrated voltage reference eases design considerations.

A programmable threshold detector allows monitoring of the signal power in the digital backend of the ADC. If the signal level exceeds the programmable threshold, the FD indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

The Subclass 1 JESD204B-based high speed serialized output data lanes can be configured to multiple configurations, depending on the sample rate and the decimation ratio. Multiple device synchronization is supported through the SYSREF_x and SYNCINB_x input pins.

ADC ARCHITECTURE

The architecture of the AD9213 consists of an input buffered, pipelined ADC. The input buffer is designed to provide a termination impedance to the analog input signal of 50 Ω. The equivalent circuit diagram of the analog input termination is shown in Figure 77. The input buffer is optimized for high linearity, low noise, and low power.

The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample. Simultaneously, the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9213 is a differential buffer. The internal common-mode voltage of the buffer is AVDD/2 (nominally 0.5 V). The clock signal alternately switches the input circuit between sample mode and hold mode.

At radio frequencies, care must be taken when designing the network between the signal source and the AD9213 inputs.

Additional loading affects bandwidth and possibly signal integrity. For more information, refer to the *Analog Dialogue* article *Transformer-Coupled Front-End for Wideband A/D Converters* (Volume 39, April 2005). In general, the specific configuration and component values depend on the application.

For best dynamic performance, the source impedances driving VIN_P and VIN_N must be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

Differential Input Configurations

There are several ways to drive the AD9213, either actively or passively. However, optimal performance is achieved by driving the analog input differentially.

For applications where SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration, because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9213.

For low to midrange frequencies, a double balun or double transformer network is recommended for optimal performance of the AD9213. For higher frequencies, remove some of the front-end passive components to ensure wideband operation.

Input Common Mode

The analog inputs of the AD9213 are internally biased to the common mode (0.50 V) by default.

In dc-coupled applications, the V_{CM} of the signal source must be biased to 0.50 V to ensure proper ADC operation. For these applications, the internal biasing of the input buffer must be disabled, and the dc offset nulling must also be disabled.

The following is pseudo code for the register writes to configure the input buffer for dc coupling.

For dc coupling, without using the VCM output pin, make the following writes: Register 0x1617 = 0x01, dc coupling mode, nulling disabled, and Register 0x151A = 0x00, internal biasing disabled, VCM output disabled.

For DC coupling, with the VCM output pin enabled, make the following writes: Register 0x1617 = 0x01, dc coupling mode, nulling disabled, and Register 0x151A = 0x02, internal biasing disabled, VCM output enabled (for providing VCM level to a driver amplifier).

The VCM output can be used to set the VCM of an amplifier driving AD9213. The VCM output buffer has a series output resistance of 100 Ω. A load on the VCM pin reduces the output voltage, which must be accounted for when loading the VCM output. The VCM output is not intended to drive high fanout, multiple load applications.

See Figure 22 and Figure 54 for information regarding variation in typical performance with respect to the V_{CM}.

Input Overvoltage Clamp

The AD9213 has an on-chip overvoltage clamp placed differentially across the ADC analog inputs to protect the input buffer of the device from large voltage excursions, as shown in Figure 89. During an overvoltage event, this N-type metal-oxide semiconductor (NMOS) clamp effectively shorts the on-chip, 50 Ω, differential input termination, attenuating the input level. The clamping circuit detects differential overvoltage, but does not sense the input V_{CM}. The clamp attenuation is at its maximum at $f_{IN} < 250$ MHz. When the $f_{IN} > 250$ MHz, clamp circuit attenuation levels are lower. Higher input frequencies result in a higher clamp threshold and a higher clamped input level.

Adding board-level circuitry to protect the ADC inputs from periodic, large voltage excursions often compromises system performance. This built in clamp allows increased typical input voltage levels and improved system performance.

During an overvoltage event, the active clamp circuit reduces the on-chip, ADC input 50 Ω differential termination (load termination resistance seen by the ADC signal source).

This reduction can cause reflections back to the circuitry that drives the ADC. Ensure that the driving circuitry is not damaged by potential large signals created with these reflections.

The user must ensure system reliability at their system specific conditions.

VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the AD9213. This internal 0.5 V reference is used to set the full-scale input range of the ADC.

The user has the option of applying a reference voltage from an external source to the VREF pin. See Figure 75 for guidance regarding appropriate external references a given application.

To enable the option to apply a reference voltage from an external source, make the following writes: Register 0x1615 = 0x01, enable VREF import path, and Register 0x1616 = 0x01, enable VREF import circuit.

These registers must be written immediately prior to Step 5 described in the Startup Sequence section.

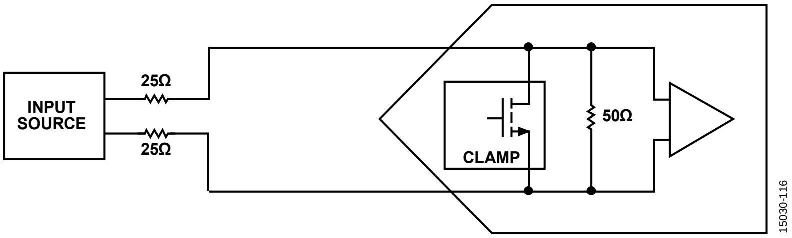


Figure 89. Input Overvoltage Clamp

CLOCK INPUT CONSIDERATIONS

The AD9213 has a low jitter clock receiver. For optimum performance, drive the AD9213 sample clock inputs (CLK_x) with a differential signal. This signal is typically ac-coupled to the CLK_x pins via a transformer or clock drivers. These pins are biased internally and require no additional external biasing.

Clock Jitter

High speed, high resolution ADCs are sensitive to the quality of the clock signal.

The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated with the following equation:

$$SNR = 20 \times \log 10 \, (2 \times \pi \times f_A \times t_J)$$

In this equation, the rms aperture jitter represents the root sum square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications.

Higher frequencies are increasingly sensitive to jitter (see Figure 90).

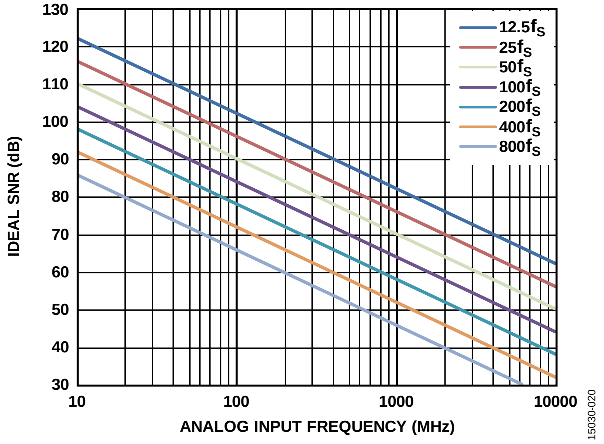


Figure 90. Ideal SNR vs. Analog Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter can affect the dynamic range of the AD9213. Separate power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. If the clock is generated from another type of source (by gating, dividing, or other methods), retime the clock by the original clock at the last step. Refer to the AN-501 Application Note and the AN-756 Application Note for more information about jitter performance as it relates to ADCs.

Power-Down/Standby Mode

The AD9213 has a PDWN pin that can be used to configure the device in power-down or standby mode.

Temperature Diode and Sensor

A thermal monitoring unit (TMU) is designed into the AD9213. The die temperature can be read by SPI as described in the TMU section.

The AD9213 also contains a diode-based temperature sensor for measuring the temperature of the die. This diode can be used in conjunction with external support components to serve as a coarse temperature sensor to monitor the internal die temperature.

TMU

The AD9213 contains a TMU that functions as a digital thermometer. The TMU is comprised of five sensors placed at different chip locations. The on-die temperature value is measured and digitized through an ADC.

At any given time, the value from the sensor with the highest temperature is stored in Register 0x1609, Bits[7:0] and Register 0x160A, Bits[7:0]. These values combine to give a 16-bit maximum temperature word. Similarly, the value from the sensor with the lowest temperature is stored in Register 0x160D, Bits[7:0] and Register 0x160E, Bits[7:0], and these values combine to give a 16-bit minimum temperature word.

The nine MSBs of each 16-bit temperature word are the integer portion of the die temperature in twos complement. The seven LSBs represent the fractional portion of the temperature, that is, the digits to the right of the decimal place. For example, the most significant of the seven LSBs represents 2^{-1} and the next bit to the right is 2^{-2}.

The following procedure is an example of obtaining the value of the sensor that produces the highest temperature reading. The procedure to reading the minimum temperature is the same as the procedure to read the maximum temperature, but with different register addresses, depending on which temperature level is read.

To obtain the maximum temperature, read Register 0x1609 (maximum temperature word containing the eight LSBs) and Register 0x160A (maximum temperature word containing the eight MSBs).

For example,

1. Register 0x1609 = 0x76 = 01110110b.
2. Register 0x160A = 0x2C = 00101100b.
3. Concatenate the MSBs to the LSBs to give a 16-bit word: Register 0x2C76 = 0010110001110110b.
4. The nine MSBs of this word represent the twos complement integer value of the temperature in degrees Celsius:
   001011000 (twos complement) = 88 (decimal).
5. The seven LSBs of the 16-bit word are the fractional portion where the most significant (left most) bit value is 2^{-1}, the next is 2^{-2}, and so on. Using this convention, 1110110 = 0.92188 (decimal).

Therefore, the die temperature reported by the highest reading sensor is 88°C + 0.92188°C = 88.92188°C. The accuracy of the TMU is typically ±2°C, and the fractional portion of the temperature value has limited significance.

Table 9. TMU Register Summary

Address	Register Name	Bits	Description	Reset	Access
0x1609	MAX_TEMPERATURE_LSB	[7:0]	Bits[7:0] of maximum temperature of all temperature sensors. Q9.7 format.	0x0	R
0x160A	MAX_TEMPERATURE_MSB	[7:0]	Bits[15:8] of maximum temperature of all temperature sensors. Q9.7 format.	0x0	R
0x160D	MIN_TEMPERATURE_LSB	[7:0]	Bits[7:0] of minimum temperature of all temperature sensors. Q9.7 format.	0x0	R
0x160E	MIN_TEMPERATURE_MSB	[7:0]	Bits[15:8] of minimum temperature of all temperature sensors. Q9.7 format.	0x0	R

ADC OVERRANGE AND FAST DETECT

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overrange bit in the JESD204B outputs provides information on the state of the analog input that is of limited usefulness. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs. In addition, because input signals can have significant slew rates, the latency of this function is of major concern. Highly pipelined converters can have significant latency. The AD9213 contains fast detect circuitry to monitor the threshold and assert the FD pin.

ADC OVERRANGE

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange indicator can be embedded within the JESD204B link as a control bit (when CS > 0). The latency of this overrange indicator matches the sample latency.

The AD9213 also records any overrange condition in either of the two virtual converters (see Figure 109). The overrange status of each virtual converter is registered as a sticky bit in Register 0x623. The contents of Register 0x623 can be cleared using Register 0x624, by toggling the bits corresponding to the virtual converter to set and reset position.

FAST THRESHOLD DETECTION (FD)

The fast detect bit is immediately set whenever the absolute value of the input signal exceeds the programmable upper threshold level. The FD bit is only cleared when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This feature provides hysteresis and prevents the FD bit from excessively toggling.

Figure 91 shows the operation of the upper threshold and lower threshold registers, along with the dwell time registers.

The FD indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, located at Register 0x101 and Register 0x102. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 200 clock cycles (maximum). The approximate upper threshold magnitude is defined by

$$Upper\ Threshold\ Magnitude\ (\text{dBFS}) = 20\log(Threshold\ Magnitude/2^{11})$$

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, located at Register 0x103 and Register 0x104. The fast detect lower threshold register is an 11-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency, but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

$$Lower\ Threshold\ Magnitude\ (\text{dBFS}) = 20\log(Threshold\ Magnitude/2^{11})$$

For example, to set an upper threshold of −6 dBFS, write 0x3FF to Register 0x101 and Register 0x102. To set a lower threshold of −10 dBFS, write 0x287 to Register 0x103 and Register 0x104.

The dwell time can be programmed from 1 to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time registers, located at Register 0x105 and Register 0x106. See the Memory Map section for more details.

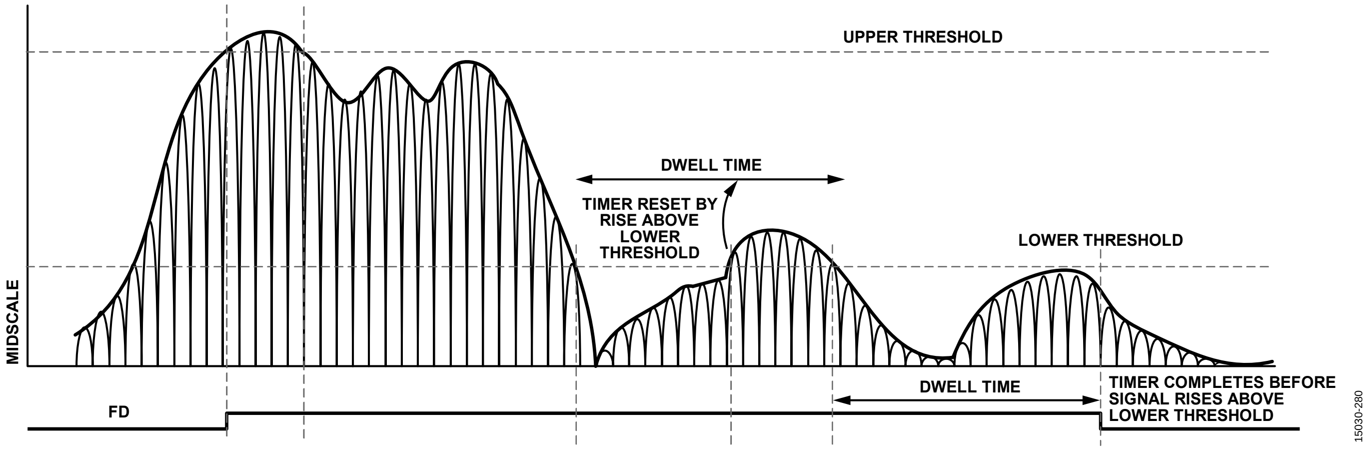


Figure 91. Threshold Settings for FD Signal

DIGITAL DOWNCONVERTER (DDC)

The AD9213 includes one DDC that provides filtering and reduce the output data rate. This digital processing section includes a numerically controlled oscillator (NCO), multiple decimating finite impulse response (FIR) filters, a gain stage, and a complex to real conversion stage. Each processing block has control lines that allow the block to be independently enabled and disabled to provide the required processing function. The DDC can be configured to output either real (I) data or complex (Q) output data.

The DDC outputs a 16-bit stream. The converter number of bits, N, is set to a default value of 12. In full bandwidth operation, the ADC outputs are the 12-bit word followed by four zeros, unless the PN tail bits or control bits are enabled.

DDC GENERAL DESCRIPTION

The DDC block extracts a portion of the full digital spectrum captured by the ADC(s). These portions are intended for intermediate frequency (IF) sampling or oversampled baseband radios requiring wide bandwidth input signals.

The DDC block contains the following signal processing stages:

- Frequency translation stage (optional)
- Filtering stage
- Gain stage (optional)
- Complex to real conversion stage (optional)

Frequency Translation Stage (Optional)

This stage consists of a phase coherent NCO and quadrature mixers that can be used for frequency translation real input signal. The phase coherent NCO allows an infinite number of frequency hops that are referenced back to a single synchronization event, and includes 16 shadow registers for fast switching applications. This stage shifts a portion of the available digital spectrum down to baseband.

Filtering Stage

After shifting down to baseband, this stage decimates the frequency spectrum using multiple low pass FIR filters for rate conversion. The decimation process lowers the output data rate, in turn reducing the output interface rate.

Gain Stage (Optional)

Due to losses associated with mixing a real input signal down to baseband, this stage compensates by adding 0 dB or 6 dB of gain to the processed signal.

Complex to Real Conversion Stage (Optional)

When real outputs are necessary, this stage converts the complex outputs back to real by performing a (f_S)/4 mixing operation and a filter operation to remove the complex component of the signal.

Figure 92 shows the detailed block diagram of the DDCs implemented in the AD9213.

Figure 93 shows an example usage of one of the four DDC channels with a real input signal and four half-band filters (HB4 + HB3 + HB2 + HB1) used. Figure 93 shows complex (decimate by 16) and real (decimate by 8) output options.

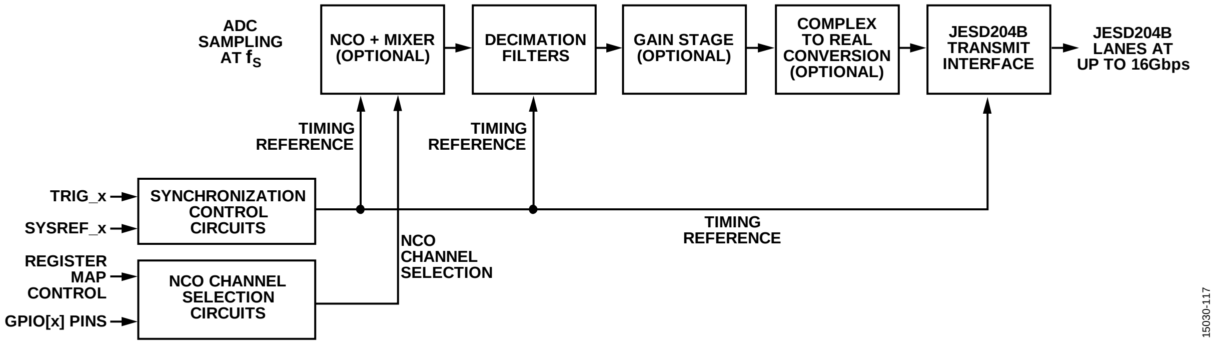


Figure 92. DDC Detailed Block Diagram

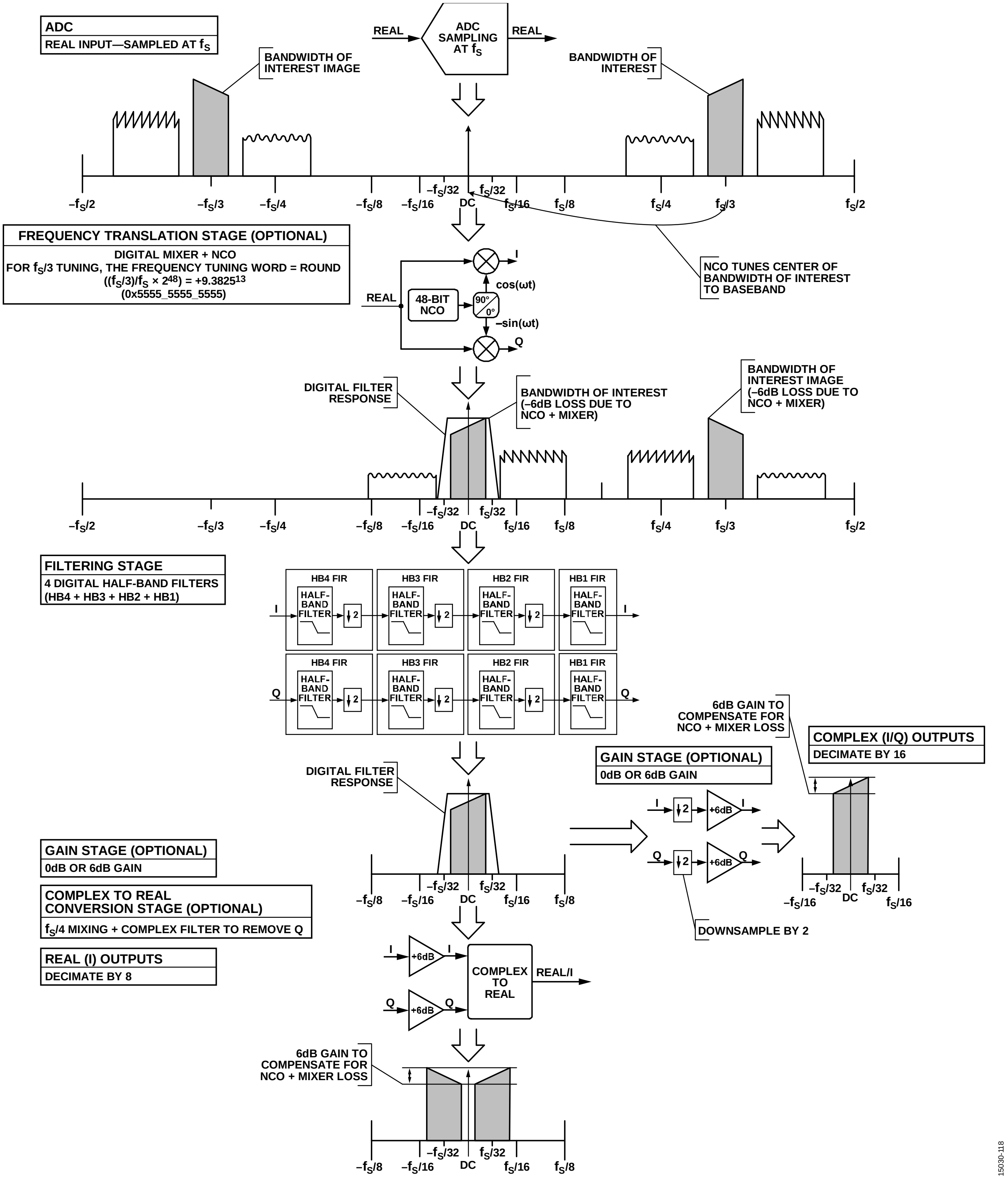


Figure 93. DDC Theory of Operation Example

DDC FREQUENCY TRANSLATION

Frequency translation is accomplished by using a 48-bit, complex NCO with a digital quadrature mixer. This stage translates a real input signal from an IF to a baseband complex digital output (carrier frequency = 0 Hz).

The frequency translation stage of each DDC can be controlled individually and supports four different IF modes using the DDC control register (Register 0x630, Bits[3:2]). The IF modes are as follows:

- Variable IF mode
- 0 Hz IF or zero IF (ZIF) mode
- f_S/4 Hz IF mode
- Test mode

Variable IF Mode

In this mode, the NCO and mixers are enabled. The NCO output frequency can be used to digitally tune the IF frequency.

ZIF Mode

In this mode, the mixers are bypassed, and the NCO is disabled.

f_S/4 Hz IF Mode

In this mode, the mixers and the NCO are enabled in special downmixing by f_S/4 mode to save power.

Test Mode

In this mode, the input samples are forced to positive full scale and the NCO is enabled. This test mode allows the NCOs to directly drive the decimation filters.

Figure 94 shows an example of the frequency translation stage.

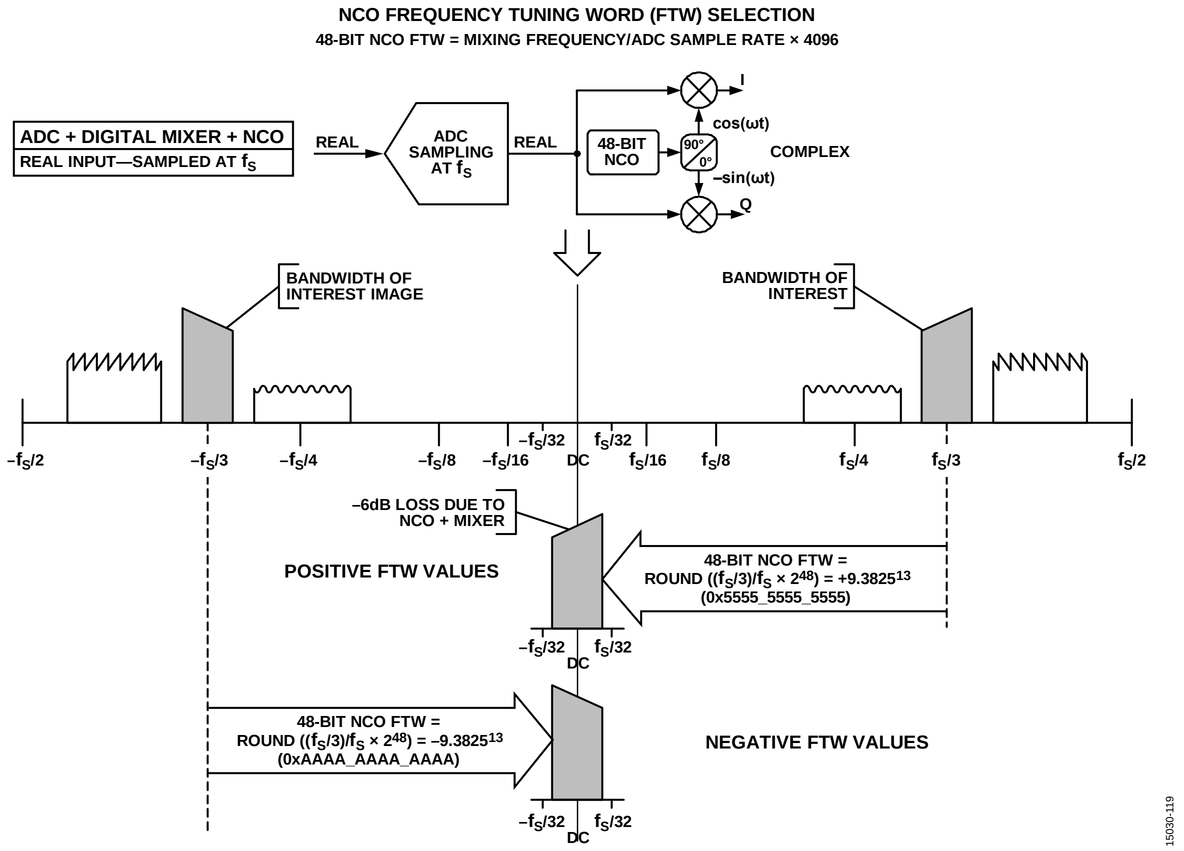


Figure 94. DDC NCO Frequency Tuning Word Selection

DDC NCO Description

The DDC contains one NCO. The NCO enables the frequency translation process by creating a complex exponential frequency ($e^{-j\omega ct}$) that can be mixed with the input spectrum to translate the desired frequency band of interest to dc, where it can be filtered by the subsequent low-pass filter blocks to prevent aliasing.

When placed in variable IF mode, the NCO supports two different additional modes: DDC NCO programmable modulus mode and DDC NCO coherent mode.

DDC NCO Programmable Modulus Mode

This mode supports >48-bit frequency tuning accuracy for applications that require exact rational (M/N) frequency synthesis at a single carrier frequency, where M is the integer representing the rational numerator of the frequency ratio, and N is the integer representing the rational denominator of the frequency ratio.

In this mode, the NCO is set up by providing the following words:

- 48-bit, frequency tuning word (FTW)
- 48-bit, Modulus A word (MAW)
- 48-bit, Modulus B word (MBW)
- 48-bit, phase offset word (POW)

DDC NCO Coherent Mode

This mode allows an infinite number of frequency hops where the phase is referenced to a single synchronization event at Time 0. This mode is useful when phase coherency must be maintained when switching between different frequency bands. In this mode, the user can switch to any tuning frequency without the need to reset the NCO. Although only one FTW is required, the NCO contains 16 shadow registers for fast-switching applications. Selection of the shadow registers is controlled by the CMOS general-purpose input/output (GPIO) pins or through the register map of the SPI. In this mode, the NCO can be set up by providing the following words:

- Up to 16 48-bit FTWs
- Up to 16 48-bit POWs
- The 48-bit MAW must be set to zero in coherent mode

Figure 95 shows a block diagram of one NCO and its connection to the rest of the design. The coherent phase accumulator block contains the logic that allows an infinite number of frequency hops.

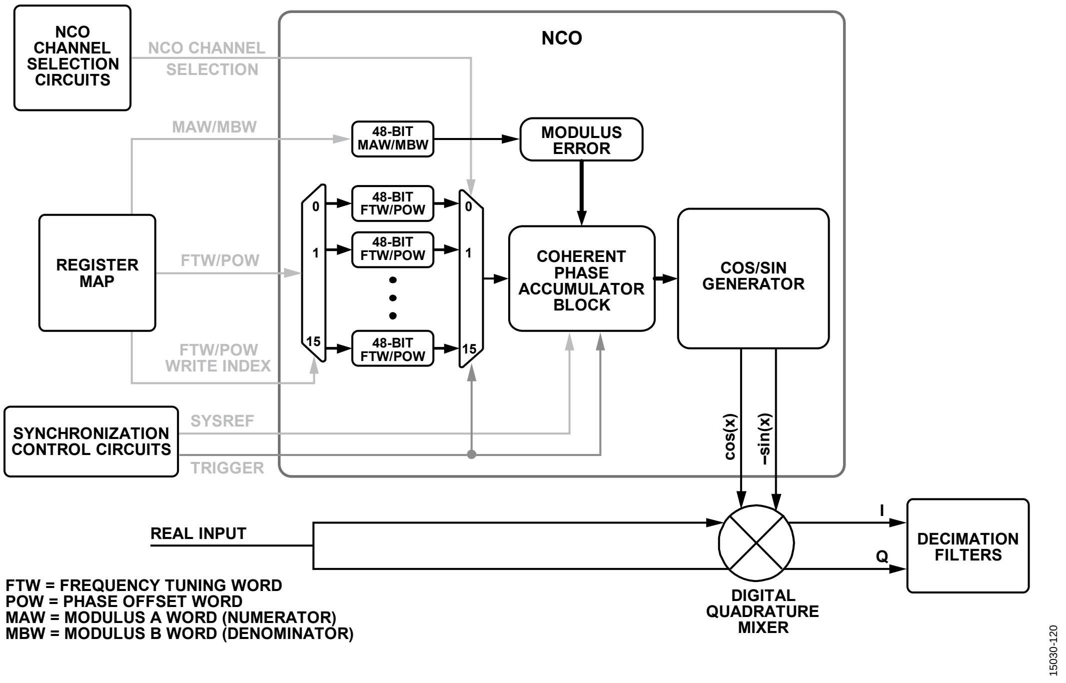


Figure 95. NCO and Mixer Block Diagram

NCO FTW, POW, MAW, and MAB Description

The NCO frequency value is determined by the following settings:

- 48-bit, twos complement number entered in the FTW
- 48-bit, unsigned number entered in the MAW
- 48-bit, unsigned number entered in the MBW

Frequencies between $-f_S/2$ and $+f_S/2$ ($+f_S/2$) are represented using the following values:

- FTW = 0x8000_0000_0000 and MAW = 0x0000_0000_0000 represents a frequency of $-f_S/2$.
- FTW = 0x0000_0000_0000 and MAW = 0x0000_0000_0000 represents dc (frequency is 0 Hz).
- FTW = 0x7FFF_FFFF_FFFF and MAW = 0x0000_0000_0000 represents a frequency of $+f_S/2$.

NCO FTW, POW, MAW, and MAB Programmable Modulus Mode Example Calculation

For programmable modulus mode, the MAW must be set to a nonzero value (not equal to 0x0000_0000_0000). This mode is only needed when frequency accuracy of >48 bits is required. One example of a rational frequency synthesis requirement that requires >48 bits of accuracy is a carrier frequency of 1/3 the sample rate. When frequency accuracy of ≤48 bits is required, coherent mode must be used (see the NCO FTW, POW, MAW, and MAB Coherent Mode section).

In programmable modulus mode, the FTW, MAW, and MBW must satisfy the following four equations (for a detailed description of the programmable modulus feature, see the AN-953 Application Note):

$$\frac{\mathrm{mod}(f_C, f_S)}{f_S} = \frac{M}{N} = \frac{FTW + \frac{MAW}{MBW}}{2^{48}} \tag{1}$$

$$FTW = \mathrm{floor}(2^{48}\frac{\mathrm{mod}(f_C, f_S)}{f_S}) \tag{2}$$

$$MAW = \mathrm{mod}(2^{48} \times M, N) \tag{3}$$

$$MBW = N \tag{4}$$

where:

mod(x) is a remainder function. For example mod(110, 100) = 10 and for negative numbers, mod(−32, +10) = −2.

f_C is the desired carrier frequency.

f_S is the ADC sampling frequency.

M is the integer representing the rational numerator of the frequency ratio.

N is the integer representing the rational denominator of the frequency ratio.

FTW is the 48-bit twos complement number representing the NCO FTW.

MAW is the 48-bit unsigned number representing the NCO MAW (must be $<2^{47}$).

MBW is the 48-bit unsigned number representing the NCO MBW.

floor(x) is defined as the largest integer less than or equal to x. For example, floor(3.6) = 3.

Equation 1 to Equation 4 apply to the aliasing of signals in the digital domain (that is, aliasing introduced when digitizing analog signals).

M and N are integers reduced to their lowest terms. MAW and MBW are integers reduced to their lowest terms. When MAW is set to zero, the programmable modulus logic is automatically disabled.

For example, if f_S is 10 GSPS and f_C is 3 1/3 GHz,

$$\frac{\mathrm{mod}\left(3\frac{1}{3}, 10\right)}{10} = \frac{M}{N} = \frac{1}{3}$$

$$FTW = \mathrm{floor}\left(2^{48}\frac{\mathrm{mod}\left(3\frac{1}{3}, 10\right)}{10}\right) = 0x5555\_5555\_5555$$

$$MAW = \mathrm{mod}(2^{48} \times 1, 3) = 0x0000\_0000\_0001$$

$$MBW = 0x0000\_0000\_0003$$

The actual carrier frequency (f_{C_ACTUAL}) can be calculated based on the following equation:

$$f_{C\_ACTUAL} = \frac{FTW + \frac{MAW}{MBW}}{2^{48}} \times f_S$$

For the previous example, f_{C_ACTUAL} is,

$$f_{C\_ACTUAL} =$$

$$\frac{0x5555\_5555\_5555 + \frac{0x0000\_0000\_0001}{0x0000\_0000\_0003}}{2^{48}} \times 10\text{ GHz} = 3\frac{1}{3}\text{ GHz}$$

A 48-bit POW is available for each NCO to create a known phase relationship between multiple chips or individual DDC channels inside the chip.

In programmable modulus mode, the deterministic phase in the NCO is not maintained when the FTW and POW are updated.

NCO FTW, POW, MAW, and MAB Coherent Mode Example Calculation

For coherent mode, the NCO MAW must be set to zero (0x0000_0000_0000). In this mode, the NCO FTW can be calculated by the following equation:

$$FTW = \mathrm{round}(2^{48}\frac{\mathrm{mod}(f_C, f_S)}{f_S}) \tag{5}$$

Where round(x) is the rounding function which rounds x to the nearest integer. For example round(3.6) = 4.

Equation 5 applies to the aliasing of signals in the digital domain (that is, aliasing introduced when digitizing analog signals). The MAW must be set to zero to use coherent mode.

When MAW is zero, the programmable modulus logic is automatically disabled.

For example, if the f_S of the ADC is 10 GSPS and the f_C is 2.6 GHz, then,

$$FTW = \text{round}\left(2^{48}\frac{\text{mod}(1.25,10)}{10}\right) = 0\text{x}2000\_0000\_0000$$

The actual carrier frequency (f_{C_ACTUAL}) can be calculated based on the following equation:

$$f_{C\_ACTUAL} = (FTW \times f_S)/2^{48}$$

For the previous example, the f_{C_ACTUAL} is

$$f_{C\_ACTUAL} = (0\text{x}2000\_0000\_0000 \times 10)/2^{48} = 1.25\text{ GHz}$$

A 48-bit POW is available for each NCO to create a known phase relationship between multiple chips or individual DDC channels inside the chip.

In coherent mode, the FTW and POW registers can be updated at any time and maintain deterministic phase results in the NCO.

NCO Channel Selection

When configured in coherent mode, only one FTW is required in the NCO. In this mode, the user can switch to any tuning frequency without the need to reset the NCO by writing to the FTW directly. However, for fast switching applications, where either all FTWs are known beforehand or it is possible to queue up the next set of FTWs, the NCO contains 16 additional shadow registers (see Figure 96). These shadow registers are referred to as the NCO channels.

Figure 96 shows a simplified block diagram of the NCO channel selection block.

Only one NCO channel is active at a time, and NCO channel selection is controlled by the CMOS GPIO pins, the register map, or the profile select timer.

Each NCO channel selector supports four different modes, as described in the following sections.

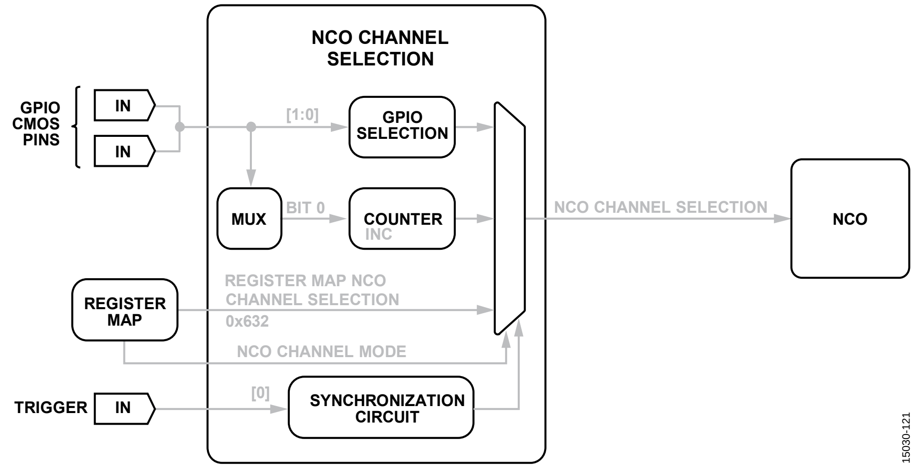


Figure 96. NCO Channel Selection Block

GPIO Level Control Mode

The GPIO[x] pins determine the exact NCO channel selected.

The following procedure must be followed to use GPIO level control for NCO channel selection:

1. Configure one or more GPIO[x] pins as an NCO channel selection input. GPIO[x] pins that are not configured as NCO channel selection are internally tied low.
   a. To use the GPIO[x] pin(s), write to Register 0x1606, Bits[3:0] to select the corresponding GPIO profile.
2. Configure the NCO channel selector in GPIO level control mode by setting Register 0x632, Bits[7:4] to 0x1 through 0x5, depending on the desired GPIO[x] pin ordering.
3. Select the desired NCO channel via the GPIO[x] pins.

GPIO Edge Control Mode

Low to high transition on the GPIO[x] pin determines the exact NCO channel selected. The internal channel selection counter is reset by either SYSREF_x signal or the DDC soft reset.

The following procedure must be followed to use GPIO edge control for NCO channel selection:

1. Configure one or more GPIO[x] pins as NCO channel selection inputs.
   a. To use the GPIO[x] pin(s), write to Register 0x1606, Bits[3:0] to select the corresponding GPIO profile.
2. Configure the NCO channel selector in GPIO edge control mode by setting Bits[7:4] in the NCO control register (Register 0x632 to 0x8 through 0xB, depending on the desired GPIO[x] pin.
3. Configure the wrap point for the NCO channel selection by setting Bits[3:0] in Register 0x632. A value of 4 causes the channel selection to wrap at Channel 4 (0, 1, 2, 3, 4, 0, 1, 2, 3, 4, and so on).
4. Transition the selected GPIO[x] pin from low to high to increment the NCO channel selection.

Profile Select Timer Mode

A 32-bit profile select timer (PST) determines the exact NCO channel selected. The channel selection counter is reset by DDC soft reset.

The following procedure must be followed to use profile select timer control for NCO channel selection.

1. Configure the NCO channel selector in profile select timer mode by setting Bits[7:4] in Register 0x632 to 0xC.
2. Configure the profile select timer by setting Register 0x65F through Register 0x664. The unit of the profile select timer is encode clock.
3. Configure the wrap point for the NCO channel selection by setting Bits[3:0] in Register 0x632. A value of 4 causes the channel selection to wrap at Channel 4 (0, 1, 2, 3, 4, 0, 1, 2, 3, 4, and so on).
4. The profile select timer specifies the number of sample clock cycles between frequency hops. The NCO channel increments when the profile select timer expires.

Register Map Mode

NCO channel selection is controlled directly through the register map.

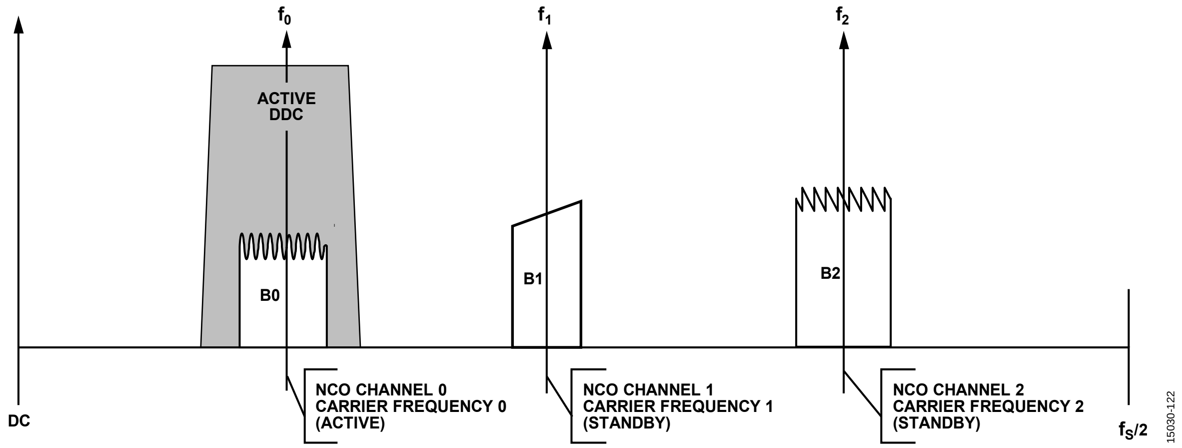


Figure 97. NCO Coherent Mode with Three NCO Channels (B0 Selected)

Figure 97 shows an example use case for coherent mode utilizing three NCO channels. In this example, NCO Channel 0 is actively downconverting Bandwidth 0 (B0) when NCO Channel 1 and NCO Channel 2 are in standby mode and tuned to Bandwidth 1 (B1) and Bandwidth 2 (B2).

The phase coherent NCO switching feature allows an infinite number of frequency hops that are all phase coherent. The initial phase of the NCO is established at Time t_0 from SYSREF_x synchronization or the signal.

Switching the NCO FTW does not affect the phase. Only one FTW is required with this feature. However, the user can use all 16 channels to queue up the next hop.

After SYSREF_x synchronization at startup, all NCOs across multiple chips are inherently synchronized.

Setting Up the Multichannel NCO Feature

The first step to configure the multichannel NCO is to program the FTWs. The AD9213 memory map has a FTW index register for the DDC. This index determines which NCO channel receives the FTW from the register map.

The following sequence describes the method for programming the FTWs:

1. Write the DDC profile (phase) update register (Register 0x633, Bit 7) to select the DDC profile (phase) update mode. The update mode can be continuous or require chip transfer.
2. Write the FTW index register (Register 0x633, Bits[3:0]).
3. Write the FTW with the desired value. The FTW register addresses are 0x634, 0x635, 0x636, 0x637, 0x638, and 0x639. This value is applied to the NCO channel index mentioned in Step 1.
4. Repeat Step 1 and Step 2 for other NCO channels.

After setting the FTWs, the user must select an active NCO channel. This selection can be done through the SPI registers, the external GPIO[x] pins, or a profile select timer.

The following sequence describes the method for selecting the active NCO channel using the SPI:

1. Set the NCO channel selection mode in Register 0x632, Bits[7:4] to 0x0 to enable SPI selection.
2. Choose the active NCO channel in Register 0x632, Bits[3:0].

The following sequence describes the method for selecting the active NCO channel using GPIO[x] CMOS pins.

1. Set NCO channel selection mode in Register 0x632, Bits[7:4] to a value between 0x1 and 0xB to enable GPIO[x] pin selection.
2. Configure the GPIO[x] pins as NCO channel selection inputs by writing to Register 0x1606.
3. NCO switching is done by externally controlling the GPIO[x] CMOS pins.

The following sequence describes the method for selecting the active NCO channel using the TRIG_x pins.

1. Set the NCO channel selection input in Register 0x602.
2. Configure the TRIG_x pin in edge control mode by writing to Bits[3:2] in Register 0x151E.
3. NCO switching is achieved by externally controlling the TRIG_x pins.

NCO Synchronization

Each NCO contains a separate PAW. The initial reset value of each PAW is set to zero and increments every clock cycle. The instantaneous phase of the NCO is calculated using the PAW, FTW, MAW, MBW, and POW.

Two methods can be used to synchronize multiple PAWs within the chip:

- Using the SPI: use the DDC soft reset bit in the DDC synchronization control register (Register 0x600, Bit 4) to reset all the PAWs in the chip. This reset is accomplished by setting the DDC soft reset bit high, and then setting this bit low. Note that this method can only be used to synchronize DDC channels within the same chip.
- Using the SYSREF_x pins: When a SYSREF_x pin is enabled in the SYSREF control registers, and the DDC synchronization is enabled in the DDC synchronization control register (Register 0x600, Bits[1:0]), the next valid edge of SYSREF_x or any subsequent edges of SYSREF_x resets all the PAWs in the chip. Note that this method can be used to synchronize DDC channels within the same chip or DDC channels within separate chips (see Table 10).

The synchronization mechanism using SYSREF_x and TRIG_x signals is shown in Figure 98.

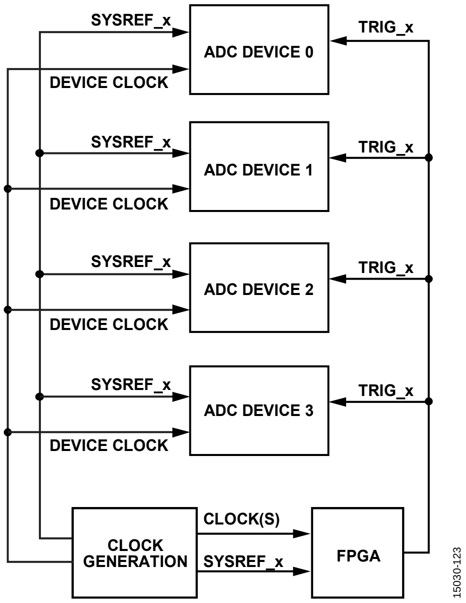


Figure 98. System Using TRIG_x and SYSREF_x for Synchronization

Table 10. Register Settings for NCO Synchronization via SYSREF_x Signal

Register Settings	Description	SYSREF_x Edge Used to Synchronize the PAWs
0x1621, Bits[3:0] ≠ 0 0x600, Bit 0 = 1 0x600, Bit 1 = 0 0x600, Bit 7 = 0	Subclass 1, DDC synchronization enable, DDC synchronization next disable, DDC synchronization TRIG_x disable	All subsequent edges of SYSREF_x signal reset all the PAWs in the chip.
0x1621, Bits[3:0] ≠ 0 0x600, Bit 0 = 1 0x600, Bit 1 = 1 0x600, Bit 7 = 0	Subclass 1, DDC synchronization enable, DDC synchronization next enable, DDC synchronization TRIG_x disable	The next valid edge of SYSREF_x signal resets all the PAWs in the chip.
0x1621, Bits[3:0] ≠ 0 0x600, Bit 0 = 0 0x600, Bit 1 = 0 0x600, Bit 7 = 1	Subclass 1, DDC synchronization disable, DDC synchronization next disable, DDC synchronization TRIG_x enable	All edges of SYSREF_x signal after TRIGGER signal reset all the PAWs in the chip.
0x1621, Bits[3:0] ≠ 0 0x600, Bit 0 = 0 0x600, Bit 1 = 1 0x600, Bit 7 = 1	Subclass 1, DDC synchronization disable, DDC synchronization next enable, DDC synchronization TRIG_x enable	The next valid edge of SYSREF_x signal after TRIGGER signal resets all the PAWs in the chip.

NCO Multichip Synchronization

In some applications, it is necessary to synchronize all the NCOs and local multiframe clocks (LMFCs) within multiple devices in a system. For applications requiring multiple NCO tuning frequencies in the system, a designer likely must generate a single SYSREF_x pulse to all devices, simultaneously.

For many systems, generating or receiving a single-shot SYSREF_x pulse on all devices is challenging because of the following factors:

- Enabling or disabling the SYSREF_x pulse is often an asynchronous event.
- Not all clock generation chips support this feature.

For these reasons, the AD9213 contains a synchronization triggering mechanism that allows the following:

- Multichip synchronization of all NCOs and LMFCs at system startup.
- Multichip synchronization of all NCOs after applying new tuning frequencies during normal operation.

NCO Multichip Synchronization at Startup

Figure 99 shows a timing diagram along with the required sequence of events for NCO multichip synchronization using triggering and the SYSREF_x signal at startup. Using this startup sequence synchronizes all the NCOs and LMFCs in the system simultaneously.

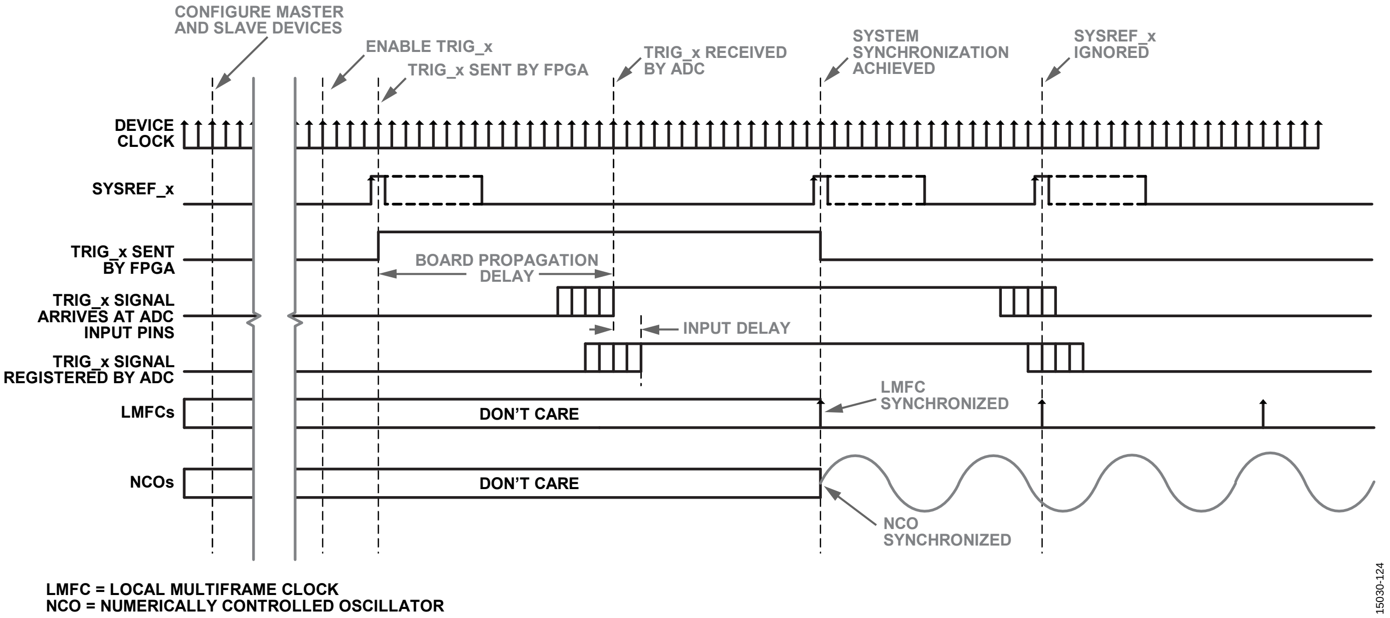


Figure 99. NCO Multichip Synchronization at Startup (Using TRIG_x and SYSREF_x)

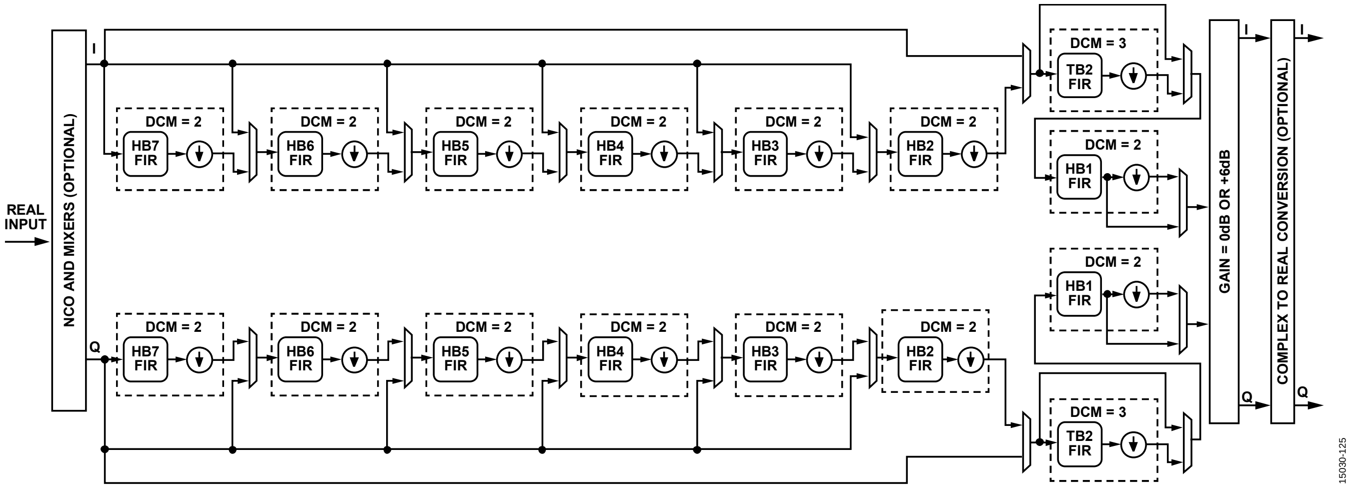


Figure 100. DDC Decimation Filter Block Diagram

DDC Mixer Description

When not bypassed (Register 0x606, Bits[3:0] ≠ 0x00), the DDC mixer performs a similar operation to an analog quadrature mixer. The DDC performs the downconversion of the input signal using the NCO frequency as a local oscillator. The input of the DDC is a real signal which means that a real mixer operation (with two multipliers) is performed.

DDC NCO, Mixer Loss, and SFDR

When mixing a real input signal down to baseband, −6 dB of loss is introduced in the signal due to filtering of the negative image. An additional −0.05 dB of loss is introduced by the NCO. The total loss of a real input signal mixed down to baseband is −6.05 dB, and it is recommended that the user compensate for this loss by enabling the 6 dB of gain in the gain stage of the DDC to recenter the dynamic range of the signal within the full scale of the output bits (see the DDC Gain Stage section for more information).

The worst case spurious signal from the NCO is >102 dBc SFDR for all output frequencies.

DDC DECIMATION FILTERS

After the frequency translation stage, there are multiple decimation filter stages used to reduce the output data rate. After the carrier of interest is tuned down to dc (carrier frequency = 0 Hz), these filters efficiently lower the sample rate and providing sufficient alias rejection from unwanted adjacent carriers around the bandwidth of interest.

Figure 100 shows a simplified block diagram of the decimation filter stage, and Table 11 describes the filter characteristics of the different FIR filter blocks.

Table 11 and Table 12 show the different filter configurations selectable by including different filters. In all cases, the DDC filtering stage provides 80% of the available output bandwidth, <±0.001 dB of pass-band ripple, and >100 dB of stop band alias rejection.

Table 11. DDC Decimation Filter (Half-Band Filter) Characteristics

Filter Name[1]	Decimation Ratio	Pass Band (rad/sec)	Stop Band (rad/sec)	Pass-Band Ripple (dB)	Stop-Band Attenuation (dB)
HB1	2	0.8 × π/2	1.2 × π/2	<±0.001	>100
HB2	2	0.4 × π/2	1.6 × π/2	<±0.001	>100
HB3	2	0.2 × π/2	1.8 × π/2	<±0.001	>100
HB4	2	0.1 × π/2	1.9 × π/2	<±0.001	>100
HB5	2	0.05 × π/2	1.95 × π/2	<±0.001	>100
HB6	2	0.025 × π/2	1.975 × π/2	<±0.001	>100
HB7	2	0.0125 × π/2	1.9875 × π/2	<±0.001	>100
TB2	3	0.8 × π/3	1.6 × π/3	<±0.001	>100

[1] All filters are FIR, low pass filters.

Table 12. DDC Filter Configurations, ADC Sample Rate = f_S

	Real (I) Output		Complex (I/Q) Outputs			
DDC Filter Configuration	Decimation Ratio	Sample Rate	Decimation Ratio	Sample Rate	Alias Protected Bandwidth	Ideal SNR Improvement (dB)[1]
HB1	1	f_S	2	$f_S/2$ (I) + $f_S/2$ (Q)	$f_S/2$ × 80%	1
HB2 + HB1	2	$f_S/2$	4	$f_S/4$ (I) + $f_S/4$ (Q)	$f_S/4$ × 80%	4
TB2 + HB1	3	$f_S/3$	6	$f_S/6$ (I) + $f_S/6$ (Q)	$f_S/6$ × 80%	5.7
HB3 + HB2 + HB1	4	$f_S/4$	8	$f_S/8$ (I) + $f_S/8$ (Q)	$f_S/8$ × 80%	7
TB2 + HB2 + HB1	6	$f_S/6$	12	$f_S/12$ (I) + $f_S/12$ (Q)	$f_S/12$ × 80%	8.8
HB4 + HB3 + HB2 + HB1	8	$f_S/8$	16	$f_S/16$ (I) + $f_S/16$ (Q)	$f_S/16$ × 80%	10
TB2 + HB3 + HB2 + HB1	12	$f_S/12$	24	$f_S/24$ (I) + $f_S/24$ (Q)	$f_S/24$ × 80%	11.8
HB5 + HB4 + HB3 + HB2 + HB1	16	$f_S/16$	32	$f_S/32$ (I) + $f_S/32$ (Q)	$f_S/32$ × 80%	13
TB2 + HB4 + HB3 + HB2 + HB1	24	$f_S/24$	48	$f_S/48$ (I) + $f_S/48$ (Q)	$f_S/48$ × 80%	14.8
HB6 + HB5 + HB4 + HB3 + HB2 + HB1	32	$f_S/32$	64	$f_S/64$ (I) + $f_S/64$ (Q)	$f_S/64$ × 80%	16
TB2 + HB5 + HB4 + HB3 + HB2 + HB1	48	$f_S/48$	96	$f_S/96$ (I) + $f_S/96$ (Q)	$f_S/96$ × 80%	17.8
HB7 + HB6 + HB5 + HB4 + HB3 + HB2 + HB1	64	$f_S/64$	128	$f_S/128$ (I) + $f_S/128$ (Q)	$f_S/128$ × 80%	19

[1] Ideal SNR improvement due to oversampling + filtering > 10log(bandwidth/$f_S/2$).

Table 13. DDC Filter Configurations (f_S = 10 GSPS)

	Real (I) Output		Complex (I/Q) Outputs		
DDC Filter Configuration	Decimation Ratio	Sample Rate (GSPS)	Decimation Ratio	Sample Rate (GSPS)	Alias Protected Bandwidth (GHz)
HB1	1	10	2	5 (I) + 5 (Q)	4
HB2 + HB1	2	5	4	2.5 (I) + 2.5 (Q)	2
TB2 + HB1	3	3.3333	6	1.6667 (I) + 1.6667 (Q)	1.3333
HB3 + HB2 + HB1	4	2.5	8	1.25 (I) + 1.25 (Q)	1
TB2 + HB2 + HB1	6	1.6667	12	0.8333 (I) + 0.8333 (Q)	0.6667
HB4 + HB3 + HB2 + HB1	8	1.25	16	0.625 (I) + 0.625 (Q)	0.5
TB2 + HB3 + HB2 + HB1	12	0.8333	24	0.4167 (I) + 0.4167 (Q)	0.3333
HB5 + HB4 + HB3 + HB2 + HB1	16	0.625	32	0.3125 (I) + 0.3125 (Q)	0.25
TB2 + HB4 + HB3 + HB2 + HB1	24	0.4167	48	0.2083 (I) + 0.2083 (Q)	0.1667
HB6 + HB5 + HB4 + HB3 + HB2 + HB1	32	0.3125	64	0.1563 (I) + 0.1563 (Q)	0.125
TB2 + HB5 + HB4 + HB3 + HB2 + HB1	48	0.2083	96	0.1042 (I) + 0.1042 (Q)	0.0833
HB7 + HB6 + HB5 + HB4 + HB3 + HB2 + HB1	64	0.1563	128	0.0781 (I) + 0.0781 (Q)	0.0625

HB7 Filter Description

The HB7 decimate by 2, half-band, low-pass, FIR filter uses a 7-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB7 filter is only used when complex outputs (decimate by 128) or real outputs (decimate by 64) are enabled. Otherwise, the filter is bypassed. Table 14 and Figure 101 show the coefficients and response of the HB7 filter.

Table 14. HB7 Filter Coefficients

HB7 Coefficient Number	Coefficient
C1, C7	−1
C2, C6	0
C3, C5	9
C4	16

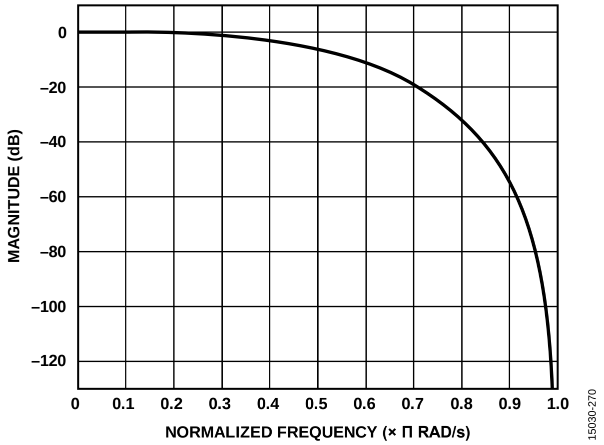


Figure 101. HB7 Filter Response

HB6 Filter Description

The HB6 decimate by 2, half-band, low-pass, FIR filter uses a 7-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB6 filter is only used when complex outputs (decimate by 64 or 128) or real outputs (decimate by 32 or 64) are enabled. Otherwise, the filter is bypassed. Table 15 and Figure 102 show the coefficients and response of the HB6 filter.

Table 15. HB6 Filter Coefficients

HB6 Coefficient Number	Coefficient
C1, C7	−1
C2, C6	0
C3, C5	9
C4	16

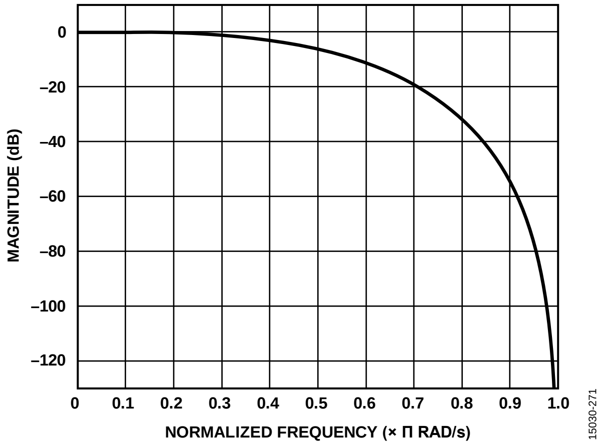


Figure 102. HB6 Filter Response

HB5 Filter Description

The HB5 decimate by 2, half-band, low-pass, FIR filter uses a 7-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption.

The HB5 filter is only used when complex outputs (decimate by 32, 64 or 128) or real outputs (decimate by 16, 32 or 64) are enabled. Otherwise, the filter is bypassed.

Table 16 and Figure 103 show the coefficients and response of the HB5 filter.

Table 16. HB5 Filter Coefficients

HB5 Coefficient Number	Coefficient
C1, C7	−128
C2, C6	0
C3, C5	1152
C4	2048

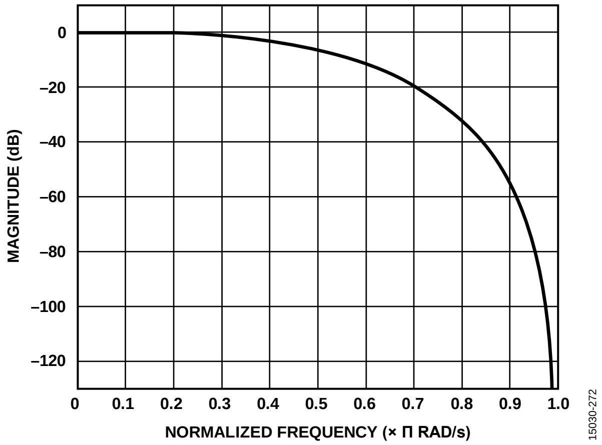


Figure 103. HB5 Filter Response

HB4 Filter Description

The HB4 decimate by 2, half-band, low-pass, FIR filter uses an 11-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption.

The HB4 filter is only used when complex outputs (decimate by 16, 32, 64 or 128) or real outputs (decimate by 8, 16, 32 or 64) are enabled. Otherwise, the filter is bypassed.

Table 17 and Figure 104 show the coefficients and response of the HB4 filter.

Table 17. HB4 Filter Coefficients

HB4 Coefficient Number	Coefficient
C1, C11	99
C2, C10	0
C3, C9	−809
C4, C8	0
C5, C7	4806
C6	8192

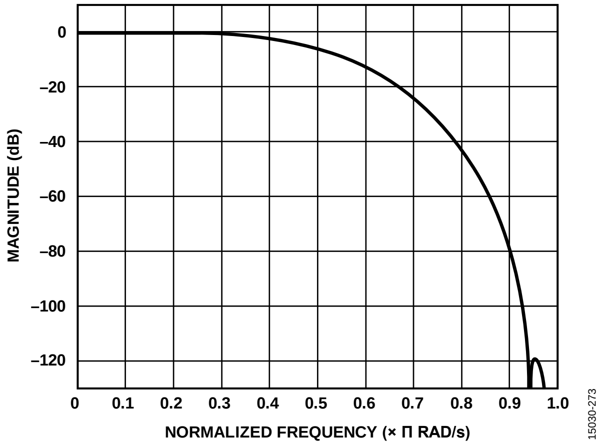


Figure 104. HB4 Filter Response

HB3 Filter Description

The HB3 decimate by 2, half-band, low-pass, FIR filter uses an 11-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption.

The HB3 filter is only used when complex outputs (decimate by 8, 16, 32, 64 or 128) or real outputs (decimate by 4, 8, 16, 32 or 64) are enabled. Otherwise, the filter is bypassed.

Table 18 and Figure 105 show the coefficients and response of the HB3 filter.

Table 18. HB3 Filter Coefficients

HB3 Coefficient Number	Coefficient
C1, C11	435
C2, C10	0
C3, C9	−3346
C4, C8	0
C5, C7	19295
C6	32,768

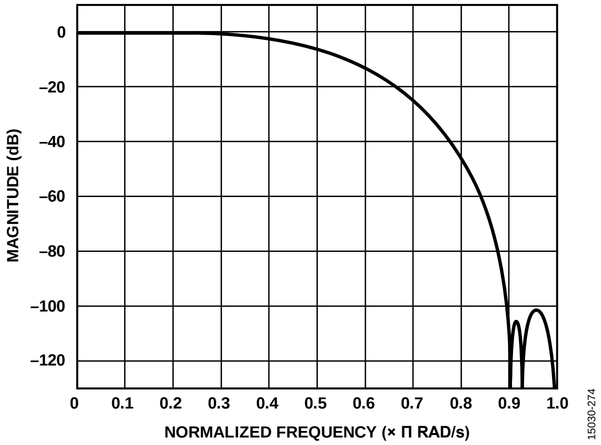


Figure 105. HB3 Filter Response

HB2 Filter Description

The HB2 decimate by 2, half-band, low-pass, FIR filter uses a 19-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption.

The HB2 filter is only used when complex outputs (decimate by 4, 8, 16, 32, 64 or 128) or real outputs (decimate by 2, 4, 8, 16, 32 or 64) are enabled. Otherwise, the filter is bypassed.

Table 19 and Figure 106 show the coefficients and response of the HB2 filter.

Table 19. HB2 Filter Coefficients

HB2 Coefficient Number	Coefficient
C1, C19	88
C2, C18	0
C3, C17	−698
C4, C16	0
C5, C15	2981
C6, C14	0
C7, C13	−9723
C8, C12	0
C9, C11	40,120
C10,	65,536

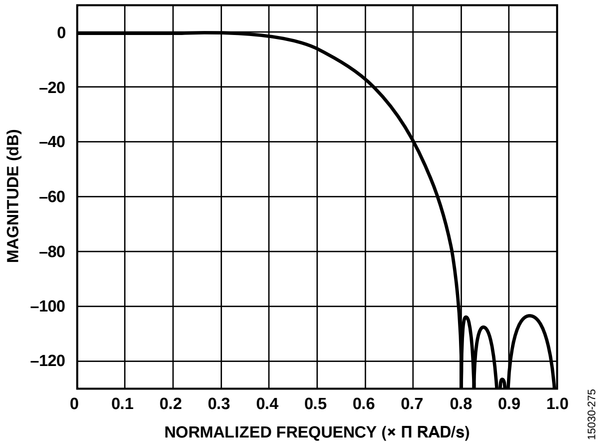


Figure 106. HB2 Filter Response

HB1 Filter Description

The HB1 and final decimate by 2, half-band, low-pass, FIR filter uses a 63-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB1 filter is always enabled and cannot be bypassed. Table 20 and Figure 107 show the coefficients and response of the HB1 filter.

Table 20. HB1 Filter Coefficients

HB1 Coefficient Number	Coefficient
C1, C63	−10
C2, C62	0
C3, C61	38
C4, C60	0
C5, C59	−102
C6, C58	0
C7, C57	232
C8, C56	0
C9, C55	−467
C10, C54	0
C11, C53	862
C12, C52	0
C13, C51	−1489
C14, C50	0
C15, C49	2440
C16, C48	0
C17, C47	−3833
C18, C46	0
C19, C45	5831
C20, C44	0
C21, C43	−8679
C22, C42	0
C23, C41	12,803
C24, C40	0
C25, C39	−19,086
C26, C38	0
C27, C37	29,814
C28, C36	0
C29, C35	−53,421
C30, C34	0
C31, C33	166,138
C32	262,144

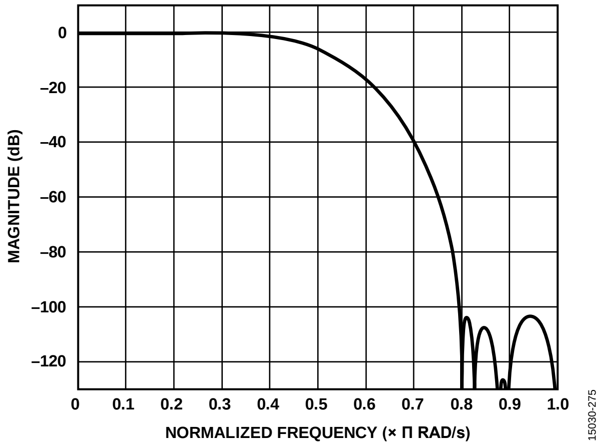


Figure 107. HB1 Filter Response

TB2 Filter Description

The TB2 decimate by 3, low-pass, FIR filter uses a 33-tap, symmetrical, fixed coefficient filter implementation. Table 21 shows the TB2 filter coefficients, and Figure 108 shows the TB2 filter response.

Table 21. TB2 Filter Coefficients

TB2 Coefficient Number	Coefficient
C1, C33	−6
C2, C32	0
C3, C31	174
C4, C30	456
C5, C29	0
C6, C28	−2010
C7, C27	−3668
C8, C26	0
C9, C25	10202
C10, C24	15932
C11, C23	0
C12, C22	−35,988
C13, C21	−53,496
C14, C20	0
C15, C19	134,175
C16, C18	283,748
C17	349,525

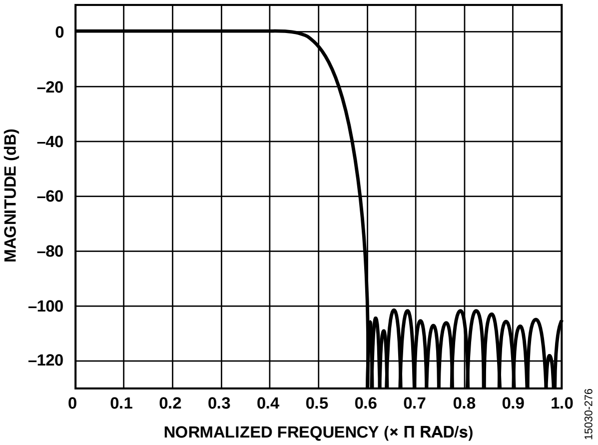


Figure 108. TB2 Filter Response

DDC GAIN STAGE

Each DDC contains an independently controlled gain stage. The gain is selectable as either 0 dB or 6 dB. When mixing a real input signal down to baseband, it is recommended that the user enable the 6 dB of gain to recenter the dynamic range of the signal within the full scale of the output bits.

DDC COMPLEX TO REAL CONVERSION

Each DDC contains an independently controlled complex to real conversion block. The complex to real conversion block reuses the last filter (HB1 FIR) in the filtering stage along with an $f_S/4$ complex mixer to upconvert the signal. The downsample by 2 portion of the HB1 FIR filter is bypassed when using the complex to real conversion stage. After upconverting the signal, the Q portion of the complex mixer is no longer needed and is dropped.

Figure 109 shows a simplified block diagram of the complex to real conversion.

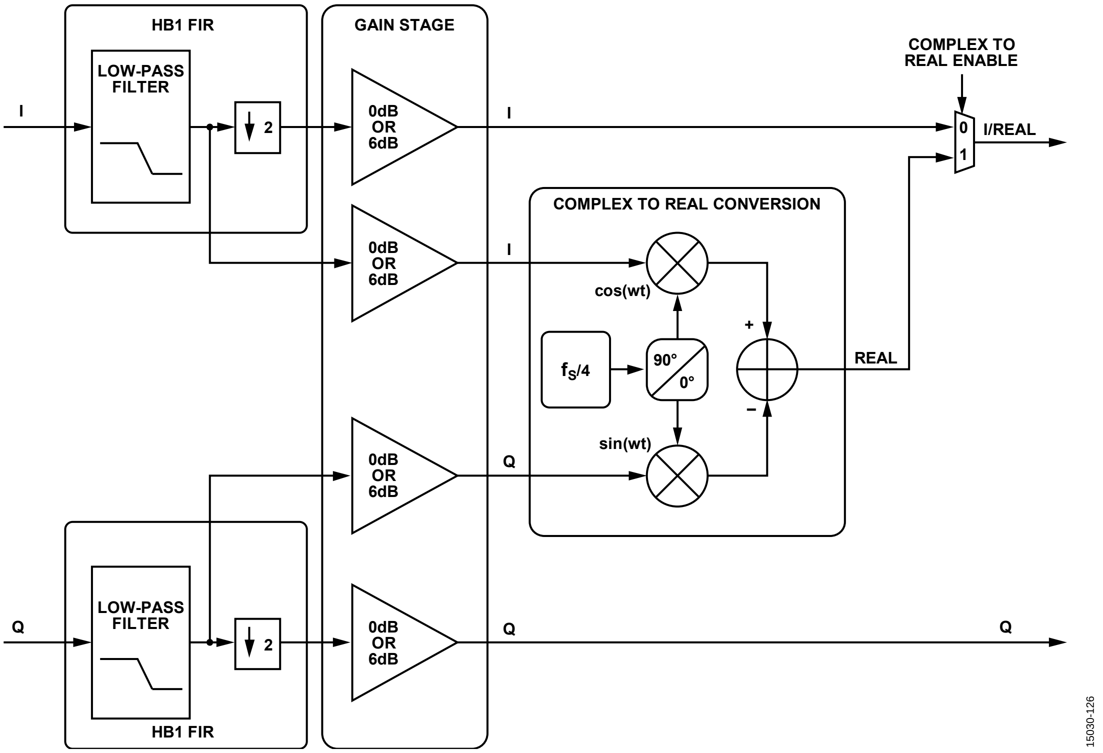


Figure 109. Complex to Real Conversion Block

DDC EXAMPLE CONFIGURATIONS

Table 22 and Table 23 describes the register settings for multiple DDC example configurations, where bandwidths are with <–0.001 dB of pass-band ripple and >100 dB of stop band alias rejection.

Table 22. Example DDC Configurations per ADC Channel Pair, Full Bandwidth Mode

Chip Application Layer	Chip Decimation Ratio (DCM)	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings
Full Bandwidth Mode	1	Don't care	50% × f_S	1	0x606 = 0x00 (full bandwidth mode) 0x607 = 0x00 (chip decimate by 1) 0x630 = 0x00 (don't care) 0x631 = 0x00 (don't care)

[1] f_S is the ADC sample rate.

Table 23. Example DDC Configurations per ADC Channel Pair, One DDC

Chip Decimation Ratio (DCM)	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings
1	Real	40% × f_S	1	Register 0x606 = 0x21. One DDC, I only selected. Register 0x607 = 0x00. Chip decimate by 1. Register 0x630 = 0x12. 6 dB gain, variable IF, real output. Register 0x631 = 0x00. HB1 filter. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
2	Complex	40% × f_S	2	Register 0x606 = 0x01. One DDC, I/Q selected. Register 0x607 = 0x01. Chip decimate by 2. Register 0x630 = 0x02. 6 dB gain, variable IF, complex output. Register 0x631 = 0x00. HB1 filter. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
	Real	20% × f_S	1	Register 0x606 = 0x21. One DDC, I only selected. Register 0x607 = 0x01. Chip decimate by 2. Register 0x630 = 0x12. 6 dB gain, variable IF, real output. Register 0x631 = 0x01. HB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
4	Complex	20% × f_S	2	Register 0x606 = 0x01. One DDC, I/Q selected. Register 0x607 = 0x02. Chip decimate by 4. Register 0x630 = 0x02. 6 dB gain, variable IF, complex output. Register 0x631 = 0x01. HB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
	Real	10% × f_S	1	Register 0x606 = 0x21. One DDC, I only selected. Register 0x607 = 0x02. Chip decimate by 4. Register 0x630 = 0x12. 6 dB gain, variable IF, real output. Register 0x631 = 0x02. HB3 + HB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
8	Complex	10% × f_S	2	0x606 = 0x01. One DDC, I/Q selected. 0x607 = 0x03. Chip decimate by 8. 0x630 = 0x02. 6 dB gain, variable IF, complex output. 0x631 = 0x02. HB3 + HB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
	Real	5% × f_S	1	Register 0x606 = 0x21. One DDC, I only selected. Register 0x607 = 0x03. Chip decimate by 8. Register 0x630 = 0x12. 6 dB gain, variable IF, real output. Register 0x631 = 0x03. HB4 + HB3 + HB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
16	Complex	5% × f_S	2	Register 0x606 = 0x01. One DDC, I/Q selected. Register 0x607 = 0x04. Chip decimate by 16. Register 0x630 = 0x02. 6 dB gain, variable IF, complex output. Register 0x631 = 0x03. HB4 + HB3 + HB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
	Real	2.5% × f_S	1	Register 0x606 = 0x21. One DDC, I only selected. Register 0x607 = 0x04. Chip decimate by 16. Register 0x630 = 0x12. 6 dB gain, variable IF, real output. Register 0x631 = 0x04. HB5 + HB4 + HB3 + HB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
32	Complex	2.5% × f_S	2	Register 0x606 = 0x01. One DDC, I/Q selected. Register 0x607 = 0x0. Chip decimate by 32. Register 0x630 = 0x02. 6 dB gain, variable IF, complex output. Register 0x631 = 0x04. HB5 + HB4 + HB3 + HB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
	Real	1.25% × f_S	1	Register 0x606 = 0x21. One DDC, I only selected. Register 0x607 = 0x05. Chip decimate by 32. Register 0x630 = 0x12. 6 dB gain, variable IF, real output. Register 0x631 = 0x05. HB6 + HB5 + HB4 + HB3 + HB2 + HB1 filters. Registers 0x634, 0x635, 0x636, 0x637, 0x638, 0x639, 0x63A, 0x63B, 0x63C, 0x63D, 0x63E, and 0x63F = FTW and POW set as required by application for DDC.

Chip Decimation Ratio (DCM)	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings
64	Complex	1.25% × f_S	2	Register 0x606 = 0x01. One DDC, I/Q selected. Register 0x607 = 0x06. Chip decimate by 64. Register 0x630 = 0x02. 6 dB gain, variable IF, complex output. Register 0x631 = 0x05. HB6 + HB5 + HB4 + HB3 + HB2 + HB1 filters). Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
	Real	0.625% × f_S	1	Register 0x606 = 0x21. One DDC; I only selected. Register 0x607 = 0x06. Chip decimate by 64. Register 0x630 = 0x12. 6 dB gain, variable IF, real output. Register 0x631 = 0x06. HB7 + HB6 + HB5 + HB4 + HB3 + HB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
128	Complex	0.625% × f_S	2	Register 0x606 = 0x01. One DDC, I/Q selected. Register 0x607 = 0x07. Chip decimate by 128. Register 0x630 = 0x02. 6 dB gain, variable IF, complex output. Register 0x631 = 0x06. HB7 + HB6 + HB5 + HB4 + HB3 + HB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
3	Real	13.33% × f_S	1	Register 0x606 = 0x21. One DDC; I only selected. Register 0x607 = 0x09. Chip decimate by 3. Register 0x630 = 0x12. 6 dB gain, variable IF, real output. Register 0x631 = 0x08. TB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
6	Complex	13.33% × f_S	2	Register 0x606 = 0x01. One DDC, I/Q selected. Register 0x607 = 0x0A. Chip decimate by 6. Register 0x630 = 0x02. 6 dB gain, variable IF, complex output. Register 0x631 = 0x08. TB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
	Real	6.667% × f_S	1	Register 0x606 = 0x21. One DDC I only selected. Register 0x607 = 0x0A. Chip decimate by 6. Register 0x630 = 0x12. 6 dB gain, variable IF, real output. Register 0x631 = 0x09. HB2 + TB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
12	Complex	6.667% × f_S	2	Register 0x606 = 0x01. One DDC, I/Q selected. Register 0x607 = 0x0B. Chip decimate by 12. Register 0x630 = 0x02. 6 dB gain, variable IF, complex output. Register 0x631 = 0x09. HB2 + TB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC
	Real	3.333% × f_S	1	Register 0x606 = 0x21. One DDC; I only selected. Register 0x607 = 0x0B. Chip decimate by 12. Register 0x630 = 0x12. 6 dB gain, variable IF, real output. Register 0x631 = 0x0A. HB3 + HB2 + TB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
24	Complex	3.333% × f_S	2	Register 0x606 = 0x01. One DDC, I/Q selected. Register 0x607 = 0x0C. Chip decimate by 24. Register 0x630 = 0x02. 6 dB gain, variable IF, complex output. Register 0x631 = 0x0A. HB3 + HB2 + TB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
	Real	1.667% × f_S	1	Register 0x606 = 0x21. One DDC, I only selected. Register 0x607 = 0x0C. Chip decimate by 24. Register 0x630 = 0x12. 6 dB gain, variable IF, real output. Register 0x631 = 0x0B. HB4 + HB3 + HB2 + TB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
48	Complex	1.667% × f_S	2	Register 0x606 = 0x01. One DDC, I/Q selected. Register 0x607 = 0x0D. Chip decimate by 48. Register 0x630 = 0x02. 6 dB gain, variable IF, complex output. Register 0x631 = 0x0B. HB4 + HB3 + HB2 + TB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.

Chip Decimation Ratio (DCM)	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings
	Real	0.8333% × f_S	1	Register 0x606 = 0x21. One DDC; I only selected. Register 0x607 = 0x0D. Chip decimate by 48. Register 0x630 = 0x12. 6 dB gain, variable IF, real output. Register 0x631 = 0x0C. HB5 + HB4 + HB3 + HB2 + TB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.
96	Complex	0.8333% × f_S	2	Register 0x606 = 0x01. One DDC, I/Q selected. Register 0x607 = 0x0E Chip decimate by 96. Register 0x630 = 0x02. 6 dB gain, variable IF, complex output.) Register 0x631 = 0x0C. HB5 + HB4 + HB3 + HB2 + TB2 + HB1 filters. Register 0x634 to Register 0x63F = FTW and POW set as required by application for DDC.

[1] f_S is the ADC sample rate.

SIGNAL MONITOR

The signal monitor block provides additional information about the signal being digitized by the ADC. The signal monitor computes the peak magnitude of the digitized signal. This information can be used to drive an AGC loop to optimize the range of the ADC in the presence of real-world signals.

The results of the signal monitor block can be obtained either by reading back the internal values from the SPI port or by embedding the signal monitoring information into the JESD204B interface as special control bits. A global, 24-bit programmable period controls the duration of the measurement. Figure 110 shows the simplified block diagram of the signal monitor block.

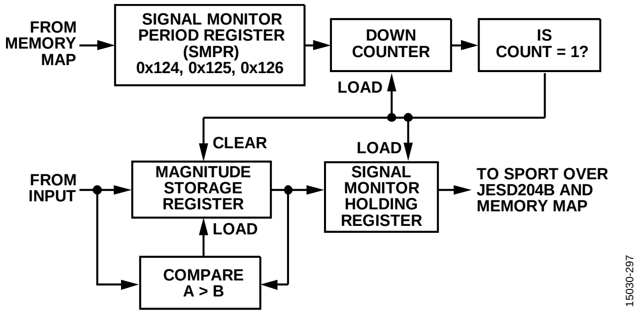


Figure 110. Signal Monitor Block

The peak detector captures the largest signal within the observation period. The detector only observes the magnitude of the signal. The resolution of the peak detector is an 11-bit value, and the observation period is 24 bits and represents converter output samples. The peak magnitude can be derived by using the following equation:

$$\textit{Peak Magnitude}\ (\text{dBFS}) = 20\log(\textit{Peak Detector Value}/2^{11})$$

The magnitude of the input port signal is monitored over a programmable time period, which is determined by the signal monitor period register (SMPR). The peak detector function is enabled by setting Bits 1 and 4 of Register 0x127 and Bit 0 of Register 0x131 in the signal monitor control register. The 24-bit SMPR must be programmed in Register 0x124 to Register 0x126 before activating this mode.

After enabling peak detection mode, the value in the SMPR is loaded into a monitor period timer, which decrements at the decimated clock rate. The magnitude of the input signal is compared with the value in the internal magnitude storage register (not accessible to the user), and the greater of the two is updated as the current peak level. The initial value of the magnitude storage register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 11-bit peak level value is transferred to the signal monitor holding register, which can be read through the memory map or output through the SPORT over the JESD204B interface. The monitor period timer is reloaded with the value in the SMPR, and the countdown restarts. In addition, the magnitude of the first input sample is updated in the magnitude storage register, and the comparison and update procedure continues.

To monitor value can be read as a Q11.9 value from Register 0x120, Register 0x121, or Register 0x122. The signal monitor runs continuously. However, this value is only updated by the user setting Bit 0 in Register 0x127. The value is stored until a subsequent update is requested by the user.

The SYSREF_x signal can be used to reset the time period counter. This allows synchronization of the signal monitor across multiple chips. This mode can be configured with Register 0x130.

SPORT OVER JESD204B

The signal monitor data can also be serialized and sent over the JESD204B interface as control bits. These control bits must be deserialized from the samples to reconstruct the statistical data. The signal control monitor function is enabled by setting Bits 0, Bit 1, and Bit 3 of Register 0x128. Figure 111 shows two different example configurations for the signal monitor control bit locations inside the JESD204B samples. A maximum of three control bits can be inserted into the JESD204B samples. However, only one control bit is required for the signal monitor. Control bits are inserted from MSB to LSB. If only one control bit is inserted, (CS = 1), only the most significant control bit is used (see Figure 111). To select the SPORT over JESD204B option, configure Register 0x620, Register 0x621, and Register 0x524. See the Memory Map section for more information on setting these bits.

Figure 112 shows the 25-bit frame data that encapsulates the peak detector value. The frame data is transmitted MSB first with five, 5-bit subframes. Each subframe contains a start bit that can be used by a receiver to validate the deserialized data. Figure 112 shows the SPORT over JESD204B signal monitor data with a monitor period timer set to 80 samples.

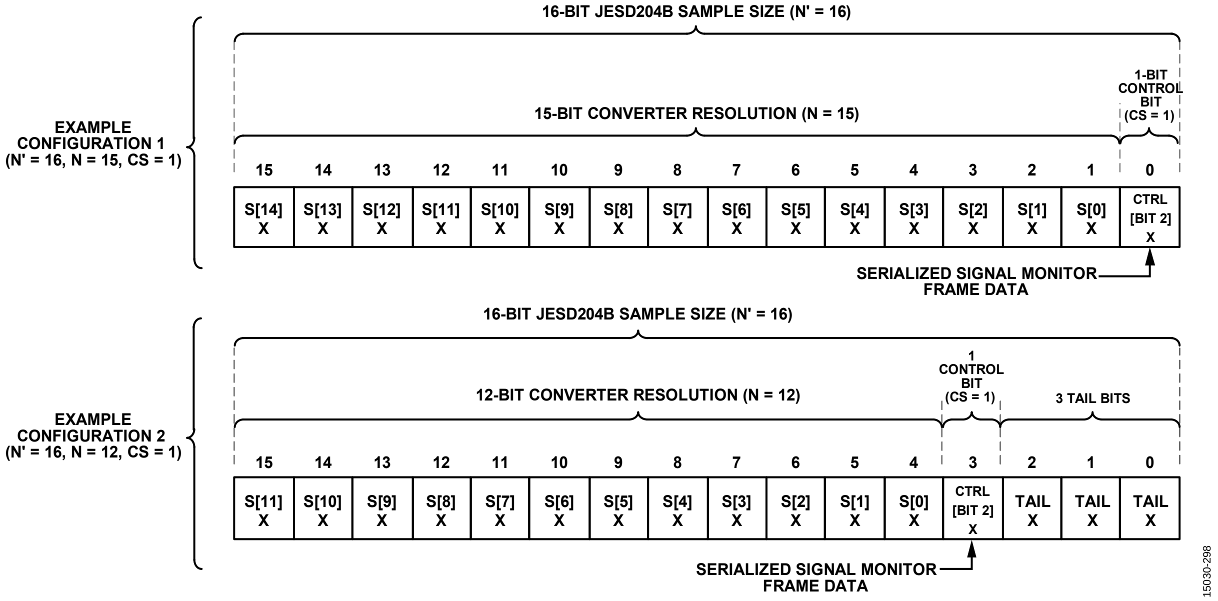


Figure 111. Signal Monitor Control Bit Location

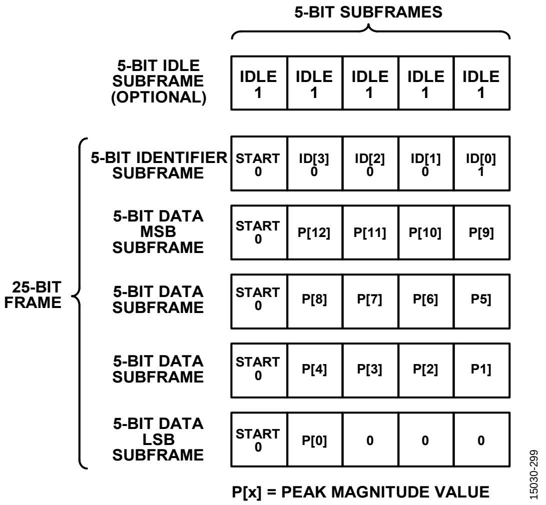


Figure 112. SPORT over JESD204B Signal Monitor Frame Data

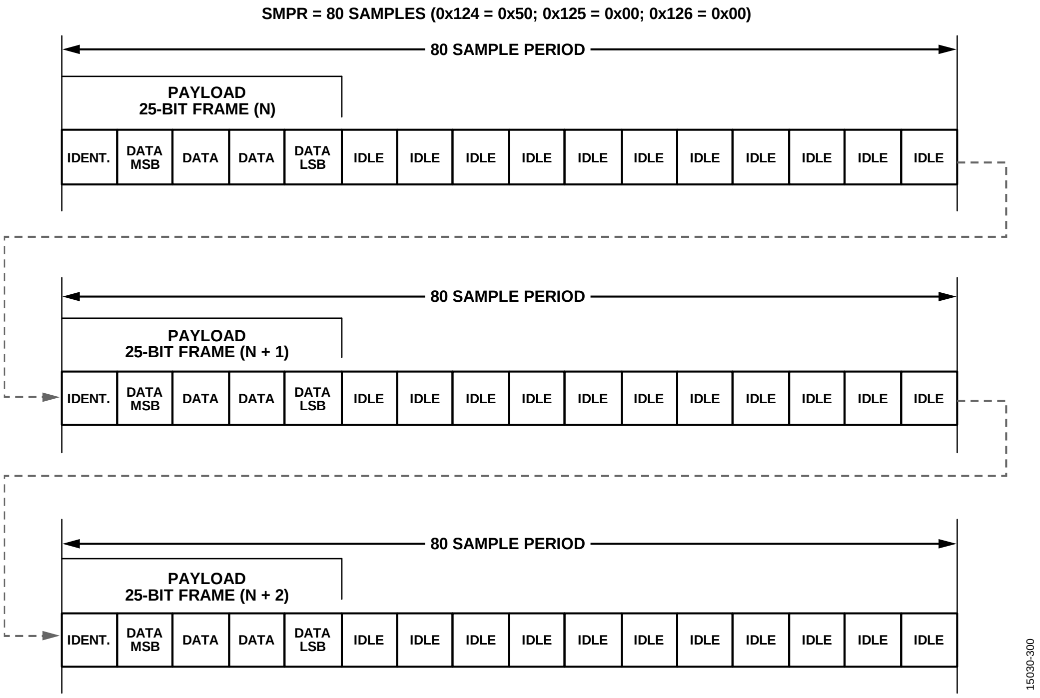


Figure 113. SPORT over JESD204B Signal Monitor Example

DIGITAL OUTPUTS

INTRODUCTION TO THE JESD204B INTERFACE

The AD9213 digital outputs are designed to the JEDEC standard JESD204B, serial interface for data converters. JESD204B is a protocol to link the AD9213 to a digital processing device over a serial interface with lane rates of up to 12.5 Gbps. The outputs of the AD9213 exceed this, being good up through 16 Gbps. The benefits of the JESD204B interface over LVDS include a reduction in required board area for data interface routing, and an ability to enable smaller packages for converter and logic devices.

JESD204B OVERVIEW

The Data Format (DFORMAT) block formats data from different sources within AD9213 and multiplexes this data to the JESD204B transmitter interface (JTx). The JESD204B data transmit block assembles the parallel data from the DFORMAT block into frames and uses 8-bit/10-bit encoding as well as optional scrambling to form serial output data. Lane synchronization is supported through the use of special control characters during the initial establishment of the link. Additional control characters are embedded in the data stream to maintain synchronization thereafter. A JESD204B receiver is required to complete the serial link. For additional details on the JESD204B interface, refer to the JESD204B standard.

The AD9213 DFORMAT block and JESD204B data transmit block maps one physical ADC or, one or two virtual converters (when DDC is enabled) over a link. A link can be configured to use up to 16 JESD204B lanes. The JESD204B specification refers to a number of parameters to define the link, and these parameters must match between the JESD204B transmitter (the AD9213 output) and the JESD204B receiver (the logic device input).

The JESD204B link is described according to the following parameters:

- L is the number of lanes per converter device (lanes per link). AD9213 value = 1, 2, 4, 8, 16, 3, 6, 12.
- M is the number of converters per converter device (virtual converters per link). AD9213 value = 1, 2.
- F is the number of octets per frame. AD9213 value = 1, 2, 4.
- N′ is the number of bits per sample (JESD204B word size). AD9213 value = 8, 12, or 16.
- N is the converter resolution. AD9213 value = 7 to 16.
- CS is the number of control bits per sample. AD9213 value = 0, 1, 2, or 3.
- K is the number of frames per multiframe, K = 32 is supported for all S.
- K = 16, 32 is supported for configurations except when S = 1 and Register 0x630, Bit 4 = 1, in which case, only K = 32 is supported.
- S is the samples transmitted per single converter per frame cycle. AD9213 value = set automatically based on L, M, F, and N′.
- HD is the high density mode. AD9213 = set automatically based on L, M, F, and N′.
- CF is the number of control words per frame clock cycle per converter device. AD9213 value = 0.

Figure 114 shows a simplified block diagram of the AD9213 JESD204B link. By default, the AD9213 is configured as one converter feeding all 16 lanes.

By default in the AD9213, the 12-bit converter word is broken into two octets (8 bits of data). Bit 11 (MSB) through Bit 4 are in the first octet. The second octet contains Bit 3 through Bit 0 (LSB) and 4 tail bits. The tail bits can be configured as zeros or a pseudorandom number sequence. The tail bits can also be replaced with control bits indicating overrange, SYSREF_x, or fast detect output.

The two resulting octets can be scrambled. Scrambling is optional. However, it is recommended to avoid spectral peaks when transmitting similar digital data patterns. The scrambler uses a self-synchronizing, polynomial-based algorithm defined by the equation $1 + x^{14} + x^{15}$. The descrambler in the receiver is a self-synchronizing version of the scrambler polynomial.

The two octets are then encoded with an 8-bit/10-bit encoder. The 8-bit/10-bit encoder works by taking eight bits of data (an octet) and encoding them into a 10-bit symbol. Figure 115 shows how the 12-bit data is taken from the ADC, how the tail bits are added, how the two octets are scrambled, and how the octets are encoded into two 10-bit symbols. Figure 115 shows the default data format.

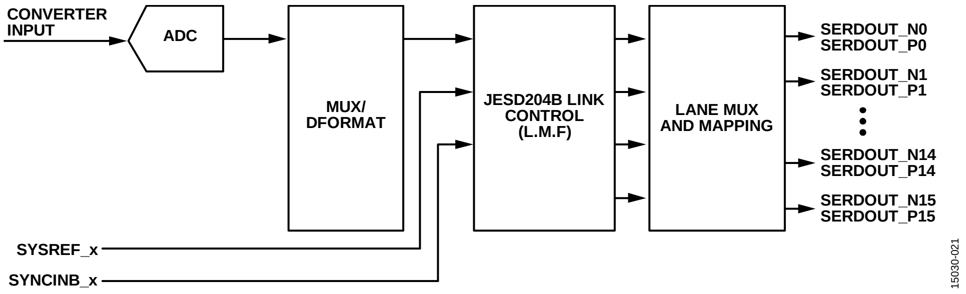


Figure 114. Transmit Link Simplified Block Diagram Showing Full Bandwidth Mode (Register 0x606 = 0x00)

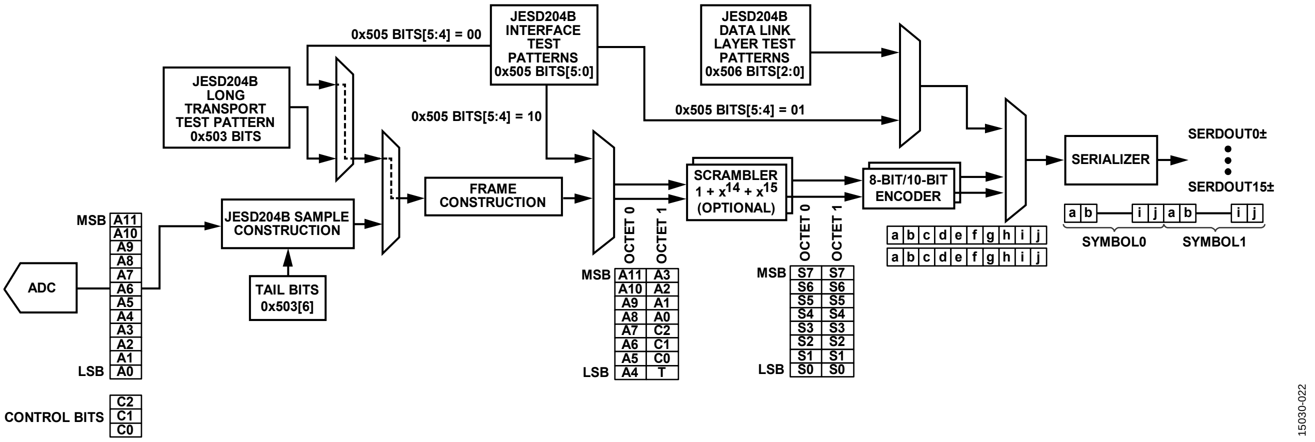


Figure 115. ADC Output Datapath Showing Data Framing (Conceptual Diagram)

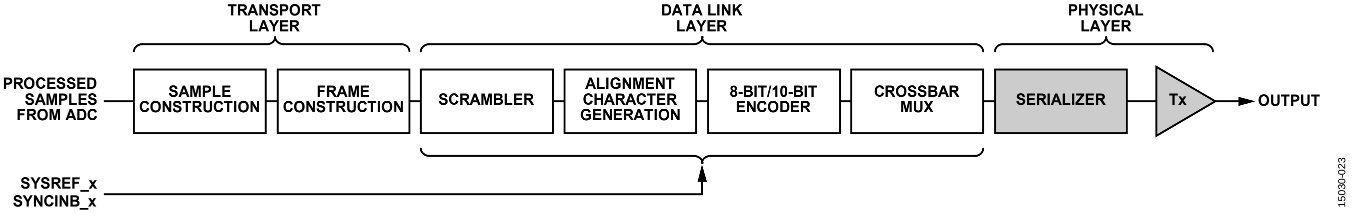


Figure 116. Data Flow

FUNCTIONAL OVERVIEW

The block diagram in Figure 116 shows the flow of data through the JESD204B hardware from the sample input to the physical output. The processing can be divided into layers that are derived from the open source initiative (OSI) model widely used to describe the abstraction layers of communications systems. These layers are the transport layer, data link layer, and physical layer (serializer and output driver).

Transport Layer

The transport layer handles packing the data (consisting of samples and optional control bits) into JESD204B frames that are mapped to 8-bit octets. These octets are sent to the data link layer. The transport layer mapping is controlled by rules derived from the link parameters. Tail bits are added to fill gaps where required.

The following equation can be used to determine the number of tail bits within a sample (JESD204B word):

$$T = N' - N - CS$$

Data Link Layer

The data link layer is responsible for the low level functions of passing data across the link. These include optionally scrambling the data, inserting control characters for multichip synchronization/lane alignment/monitoring, and encoding 8-bit octets into 10-bit symbols. The data link layer is also responsible for sending the initial lane alignment sequence (ILAS), which contains the link configuration data used by the receiver to verify the settings in the transport layer.

Physical Layer

The physical layer consists of the high speed circuitry clocked at the serial clock rate. In this layer, parallel data is converted into one through sixteen lanes of high speed differential serial data.

JESD204B LINK ESTABLISHMENT

The AD9213 JESD204B transmitter interface operates in Subclass 1 as defined in the JEDEC Standard 204B (July 2011 specification). The link establishment process is divided into the following steps: code group synchronization and SYNCINB_x, initial lane alignment sequence, and user data and error correction.

Code Group Synchronization (CGS) and SYNCINB_x

The CGS is the process by which the JESD204B receiver finds the boundaries between the 10-bit symbols in the stream of data. During the CGS phase, the JESD204B transmit block transmits /K28.5/ characters. The receiver must locate /K28.5/ characters in its input data stream using clock and data recovery (CDR) techniques.

The receiver issues a synchronization request by asserting the SYNCINB_x pin of the AD9213 low. The JESD204B transmitter then begins sending /K/ characters. When the receiver has synchronized, it waits for the correct reception of at least four consecutive /K/ symbols. It then deasserts the SYNCINB_x. The AD9213 then transmits an ILAS on the following LMFC boundary.

For more information on the code group synchronization phase, refer to the JEDEC Standard JESD204B, July 2011, Section 5.3.3.1.

The SYNCINB_x pin operation can also be controlled by the SPI. The SYNCINB_x signal is a differential, dc-coupled LVDS mode signal by default but can also be driven single-ended. For more information on configuring the SYNCINB_x pin operation, refer to Register 0x508.

The SYNCINB_x pins can also be configured to run in CMOS (single-ended) mode, by setting Bit[5] in Register 0x508. When running SYNCINB_x in CMOS mode, connect the CMOS SYNCINB_x signal to Pin F1 (SYNCINB_P) and leave Pin G1 (SYNCINB_N) floating.

ILAS

The ILAS phase follows the CGS phase and begins on the next LMFC boundary. The ILAS consists of four multiframes, with an /R/ character marking the beginning and an /A/ character marking the end. The ILAS begins by sending an /R/ character followed by 0 to 255 ramp data for one multiframe. On the second multiframe, the link configuration data is sent, starting with the third character. The second character is a /Q/ character to confirm that the link configuration data follows. All undefined data slots are filled with ramp data. The ILAS sequence is never scrambled.

The ILAS sequence construction is shown in Figure 117. The four multiframes include the following:

- Multiframe 1. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 2. Begins with an /R/ character followed by a /Q/ character (/K28.4/), followed by link configuration parameters over 14 configuration octets (see Table 24) and ends with an /A/ character. Many of the parameter values are of the value – 1 notation.
- Multiframe 3. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 4. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).

User Data and Error Detection

After the ILAS is complete, the user data is sent. Normally, within a frame, all characters are considered user data. However, to monitor the frame clock and multiframe clock synchronization, there is a mechanism for replacing characters with /F/ or /A/ alignment characters when the data meets certain conditions. These conditions are different for unscrambled and scrambled data. The scrambling operation is enabled by default, but it can be disabled using the SPI.

For scrambled data, any 0xFC character at the end of a frame is replaced by an /F/, and any 0x7C character at the end of a multiframe is replaced with an /A/. The JESD204B receiver checks for /F/ and /A/ characters in the received data stream and verifies that they only occur in the expected locations. If an unexpected /F/ or /A/ character is found, the receiver handles the situation by using dynamic realignment or asserting the SYNCINB_x signal for more than four frames to initiate a resynchronization. For unscrambled data, if the final character of two subsequent frames are equal, the second character is replaced with an /F/ if it is at the end of a frame, and an /A/ if it is at the end of a multiframe.

Insertion of alignment characters can be modified using the SPI. The frame alignment character insertion (FACI) is enabled by default. More information on the link controls is available in the Memory Map section, Register 0x503.

8-Bit/10-Bit Encoder

The 8-bit/10-bit encoder converts 8-bit octets into 10-bit symbols and inserts control characters into the stream when needed. The control characters used in JESD204B are shown in Table 24. The 8-bit/10-bit encoding ensures that the signal is dc balanced by using the same number of ones and zeros across multiple symbols.

The 8-bit/10-bit interface has options that can be controlled via the SPI. These operations include bypass and invert. These options are troubleshooting tools for the verification of the digital front end (DFE). See the Memory Map section, Register 0x504, Bits[2:1] for information on configuring the 8-bit/10-bit encoder.

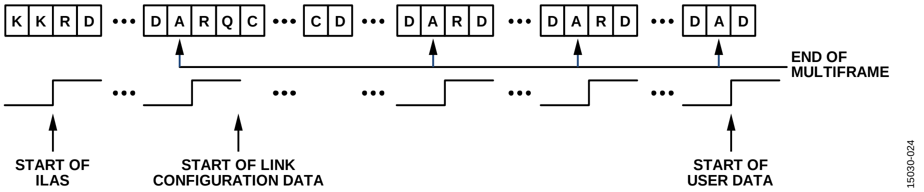


Figure 117. Initial Lane Alignment Sequence

Table 24. AD9213 Control Characters Used in JESD204B

Abbreviation	Control Symbol	8-Bit Value	10-Bit Value, RD[1] = −1	10-Bit Value, RD[1] = +1	Description
/R/	/K28.0/	000 11100	001111 0100	110000 1011	Start of multiframe
/A/	/K28.3/	011 11100	001111 0011	110000 1100	Lane alignment
/Q/	/K28.4/	100 11100	001111 0100	110000 1101	Start of link configuration data
/K/	/K28.5/	101 11100	001111 1010	110000 0101	Group synchronization
/F/	/K28.7/	111 11100	001111 1000	110000 0111	Frame alignment

[1] RD means running disparity.

PHYSICAL LAYER (DRIVER) OUTPUTS

Digital Outputs, Timing, and Controls

The AD9213 physical layer consists of drivers that are defined in the JEDEC Standard JESD204B, July 2011. The differential digital outputs are powered up by default. The drivers use a dynamic 100 Ω internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver input to result in a nominal 300 mV p-p swing at the receiver (see Figure 118). Alternatively, single-ended 50 Ω termination can be used. When single-ended termination is used, the termination voltage is JVDD/2.

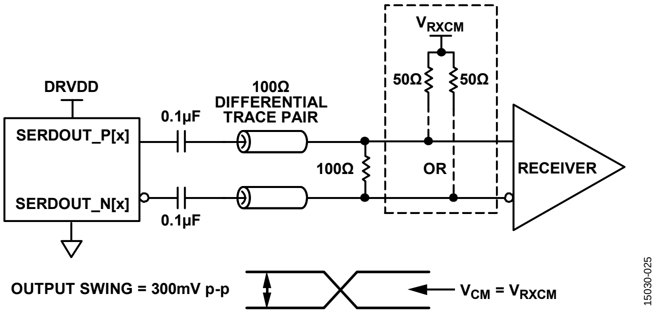


Figure 118. AC-Coupled Digital Output Termination Example

The AD9213 digital outputs can interface with custom ASICs and FPGA receivers, providing superior switching performance in noisy environments. Single point-to-point network topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver inputs as possible.

If there is no far-end receiver termination, or if there is poor differential trace routing, timing errors can result. To avoid such timing errors, it is recommended that the trace length be less than six inches, and that the differential output traces be close together and of equal lengths.

Figure 119 shows examples of the digital output data eye, time interval error (TIE) jitter histogram, and bathtub curve for one AD9213 lane running at 16Gbps. The format of the output data is twos complement by default. To change the output data format, see the Memory Map section (Register 0x622).

De-emphasis

De-emphasis enables the receiver eye diagram mask to be met in conditions where the interconnect insertion loss does not meet the JESD204B specification. Use the de-emphasis feature only when the receiver is unable to recover the clock due to excessive insertion loss. Under normal conditions, it is disabled to conserve power. Additionally, enabling and setting too high a de-emphasis value on a short link can cause the receiver eye diagram to fail. Use the de-emphasis setting with caution because it can increase electromagnetic interference (EMI). See the Memory Map section (Register 0x5BA to Register 0x5C1 in Table 36) for more details.

PLL

The PLL generates the serializer clock, which operates at the JESD204B lane rate. The status of the PLL lock can be checked in the PLL locked status bit (Register 0x501, Bit 7). This read only bit lets the user know if the PLL has achieved a lock for the specific setup. The JESD204B lane rate control, Bits[3:0] of Register 0x500, must be set to correspond with the lane rate.

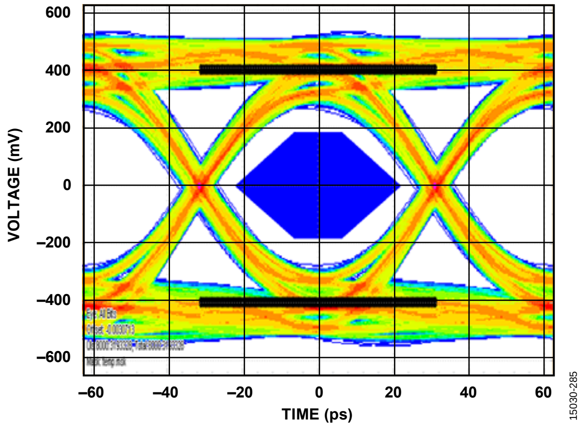


Figure 119. Digital Outputs Data Eye, External 100 Ω Terminations at 16 Gbps

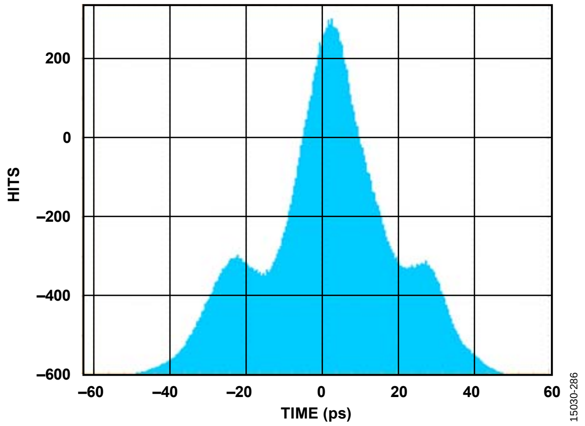


Figure 120. Digital Outputs Histogram, External 100 Ω Terminations at 16 Gbps

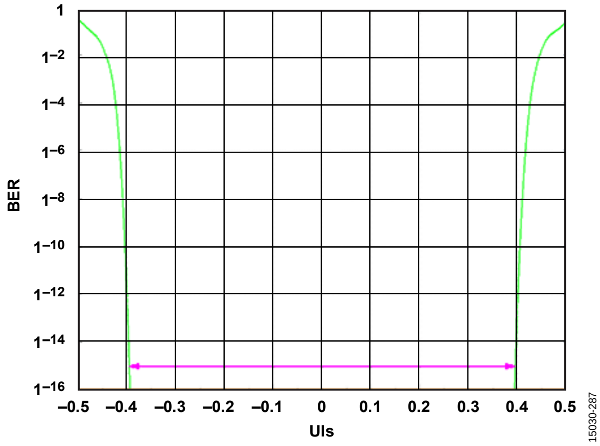


Figure 121. Digital Outputs Bathtub Curve, External 100 Ω Terminations at 16 Gbps

SETTING UP THE AD9213 DIGITAL INTERFACE

The AD9213 has one JESD204B link. The device offers an easy way to set up the JESD204B link through the JESD204B quick configuration register (Register 0x502). The serial outputs (SERDOUT0_x to SERDOUT15_x) are considered to be part of one JESD204B link. The basic parameters that determine the link setup are:

- Number of lanes per link (L)
- Number of converters per link (M)
- Number of octets per frame (F)

If the internal DDC is used for on-chip digital processing, M represents the number of virtual converters.

The maximum lane rate allowed by the AD9213 is 16 Gbps. The lane line rate is related to the JESD204B parameters using the following equation:

$$Lane\ Line\ Rate = \frac{M \times N' \times \left(\frac{10}{8}\right) \times f_{OUT}}{L}$$

where f_{OUT} is the f_{ADC_CLOCK} divided by the decimation ratio.

The DCM is the parameter programmed in Register 0x631.

The following steps can be used to configure the output:

1. Power down the link.
2. Select JESD204B link configuration options.
3. Configure detailed options.
4. Set output lane mapping (optional).
5. Set additional driver configuration options (optional).
6. Power up the link.

If the lane line rate calculated is less than 6.8 Gbps, select the low line rate option by programming a value of 0x01 to Register 0x500.

Table 25, Table 26, and Table 27 show the JESD204B output configurations supported for N′ = 16, N′ = 12 and N′ = 8 for a given number of virtual converters. Take care to ensure that the serial line rate for a given configuration is within the supported range of 1.7 Gbps to 16 Gbps.

JESD204B Transport Layer Settings

See the JESD204B Overview section for details regarding the transport layer information listed in Table 25, Table 26, and Table 27.

Serial Line Rates

In Table 25, Table 26, and Table 27, the serial line rates are as follows:

- f_{IN} = ADC input sample rate
- CDR = chip decimation ratio
- F_{OUT} = output sample rate = f_{IN}/CDR.
- SLR = JESD204B serial line rate

The following equations must be met due to internal clock divider requirements:

- SLR ≥ 1700 Mbps and SLR ≤ 16,000 Mbps.
- $SLR/40 \leq f_{IN}$
- $20 \times CDR \times f_{OUT} / SLR \leq 512$
- When the SLR is ≤16,000 Mbps and >13,600 Mbps, JTX_LOW_LINE_RATE, Register 0x500, Bits[3:0] must be set to 0x3.
- When the SLR is ≤13,600 Mbps and ≥6800 Mbps, JTX_LOW_LINE_RATE, Register 0x500, Bits[3:0] must be set to 0x0.
- When the SLR is <6800 Mbps and ≥3400 Mbps, JTX_LOW_LINE_RATE, Register 0x500, Bits[3:0]must be set to 0x1.
- When the SLR is <3400 Mbps and ≥1700 Mbps, JTX_LOW_LINE_RATE, Register 0x500, Bits[3:0]must be set to 0x5.

K Settings

In Table 25, Table 26, and Table 27, the number of samples per converter per frame cycle, S, is calculated as follows:

- S = 8 × F × L/(N' × M)
- K = 32 is supported for all S
- K = 16, 32 is supported for configurations except when S = 1 and Register 0x630, Bit 4 = 1 in which case, only K = 32 is supported.

Table 25. JESD204B Output Configurations (N' = 16)

No. of Virtual Converters Supported (Same Value as M)	JESD204B Serial Line Rate[1]	DCM Supported[2]	JESD204B Transport Layer Settings[3]								
			L	M	F	S	HD	N	N'	CS	K
1	20 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	1	1	2	1	0	8 to 16	16	0 to 3	See the K Settings section
	10 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	2	1	1	1	1	8 to 16	16	0 to 3	See the K Settings section
	10 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	2	1	2	2	0	8 to 16	16	0 to 3	See the K Settings section
	5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	4	1	1	2	1	8 to 16	16	0 to 3	See the K Settings section
	5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	4	1	2	4	0	8 to 16	16	0 to 3	See the K Settings section
	2.5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	8	1	1	4	1	8 to 16	16	0 to 3	See the K Settings section
	2.5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	8	1	2	8	0	8 to 16	16	0 to 3	See the K Settings section
	1.25 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32	16	1	1	8	1	8 to 16	16	0 to 3	See the K Settings section
	1.25 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32	16	1	2	16	0	8 to 16	16	0 to 3	See the K Settings section
2	40 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	1	2	4	1	0	8 to 16	16	0 to 3	See the K Settings section
	20 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	2	2	2	1	0	8 to 16	16	0 to 3	See the K Settings section
	10 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	4	2	1	1	1	8 to 16	16	0 to 3	See the K Settings section
	10 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	4	2	2	2	0	8 to 16	16	0 to 3	See the K Settings section
	5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	8	2	1	2	1	8 to 16	16	0 to 3	See the K Settings section
	5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	8	2	2	4	0	8 to 16	16	0 to 3	See the K Settings section
	2.5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	16	2	1	4	1	8 to 16	16	0 to 3	See the K Settings section
	2.5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	16	2	2	8	0	8 to 16	16	0 to 3	See the K Settings section

[1] See the JESD204B Overview section for full definitions and conditions.
[2] Due to the internal clock requirements, only certain decimation rates are supported for certain link parameters.
[3] See the JESD204B Transport Layer Settings section for full definitions.

Table 26. JESD204B Output Configurations (N’ = 12)

No. of Virtual Converters Supported (Same Value as M)	JESD204B Serial Line Rate[1]	DCM Supported[2]	JESD204B Transport Layer Settings[3]								
			L	M	F	S	HD	N	N'	CS	K
1	5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	3	1	1	2	1	8 to 12	12	0 to 3	See the K Settings section
	2.5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	6	1	1	4	1	8 to 12	12	0 to 3	See the K Settings section
	1.25 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32	12	1	1	8	1	8 to 12	12	0 to 3	See the K Settings section
2	10 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	3	2	1	1	1	8 to 12	12	0 to 3	See the K Settings section
	5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	6	2	1	2	1	8 to 12	12	0 to 3	See the K Settings section
	2.5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	12	2	1	4	1	8 to 12	12	0 to 3	See the K Settings section

[1] See the JESD204B Overview section for full definitions and conditions.
[2] Due to the internal clock requirements, only certain decimation rates are supported for certain link parameters.
[3] See the JESD204B Transport Layer Settings section for full definitions.

Table 27. JESD204B Output Configurations (N’ = 8)

No. of Virtual Converters Supported (Same Value as M)	JESD04B Serial Line Rate[1]	DCM Supported[2]	JESD204B Transport Layer Settings[3]								
			L	M	F	S	HD	N	N'	CS	K
1	10 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	1	1	1	1	0	7 to 8	8	0 to 1	See the K Settings section
	10 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	1	1	2	2	0	7 to 8	8	0 to 1	See the K Settings section
	5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	2	1	1	2	0	7 to 8	8	0 to 1	See the K Settings section
	5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	2	1	2	4	0	7 to 8	8	0 to 1	See the K Settings section
	5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	2	1	4	8	0	7 to 8	8	0 to 1	See the K Settings section
	2.5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	4	1	1	4	0	7 to 8	8	0 to 1	See the K Settings section
	2.5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	4	1	2	8	0	7 to 8	8	0 to 1	See the K Settings section
	1.25 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32	8	1	1	8	0	7 to 8	8	0 to 1	See the K Settings section
	1.25 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32	8	1	2	16	0	7 to 8	8	0 to 1	See the K Settings section
2	20 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	1	2	2	1	0	7 to 8	8	0 to 1	See the K Settings section
	10 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	2	2	1	1	0	7 to 8	8	0 to 1	See the K Settings section
	10 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	2	2	2	2	0	7 to 8	8	0 to 1	See the K Settings section
	5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	4	2	1	2	0	7 to 8	8	0 to 1	See the K Settings section
	5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	4	2	2	4	0	7 to 8	8	0 to 1	See the K Settings section
	5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	4	2	4	8	0	7 to 8	8	0 to 1	See the K Settings section
	2.5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	8	2	1	4	0	7 to 8	8	0 to 1	See the K Settings section
	2.5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	8	2	2	8	0	7 to 8	8	0 to 1	See the K Settings section
	2.5 × f_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	8	2	4	16	0	7 to 8	8	0 to 1	See the K Settings section

[1] See the JESD204B Overview section for full definitions and conditions.
[2] Due to the internal clock requirements, only certain decimation rates are supported for certain link parameters.
[3] See the JESD204B Transport Layer Settings section for full definitions.

LATENCY

END TO END TOTAL LATENCY

Total latency in the AD9213 is dependent on the chip application mode and the JESD204B configuration. For any given combination of these parameters, the latency is deterministic, however, the value of this deterministic latency must be calculated as described in the Example Latency Calculations section.

Table 28 shows the combined latency through the ADC and DSP for the different chip application modes supported by the AD9213. Table 29 shows the latency through the JESD204B block for each application mode based on the M/L ratio. For both tables, latency is typical and is in units of the encode clock. The latency through the JESD204B block does not depend on the output data type (real or complex). Therefore, data type is not included in Table 28 and Table 29.

To determine the total latency, select the appropriate ADC + DSP latency from Table 28 and add it to the appropriate JESD204B latency from Table 29.

EXAMPLE LATENCY CALCULATIONS

An example configuration with latency calculation is shown below:

- ADC application mode = full bandwidth
- Real outputs
- L = 16, M = 1, F = 1, S = 8 (JESD204B mode)
- M/L = 0.0625
- Latency = 187 encode clock periods + 180 encode clock periods = 367 encode clock periods

LMFC REFERENCED LATENCY

Some FPGA vendors may require the end user to know LMFC referenced latency to make appropriate deterministic latency adjustments. If they are required, the latency values in Table 28 and Table 29 can be used for the analog input to LMFC and LMFC to data output latency values, respectively.

Table 28. Typical Latency Through the ADC + DSP Blocks (Number of Sample Clocks)[1]

Chip Application Mode	Enabled Filters	ADC + DSP Latency (Clock Cycles)
Full Bandwidth	Not applicable	180
DCM1, Real	HB1	520
DCM2		
Complex	HB1	518
Real	HB2 + HB1	866
DCM3, Real	TB2 + HB1	1273
DCM4		
Complex	HB2 + HB1	894
Real	HB3 +HB2 + HB1	1655
DCM6		
Complex	TB2 + HB1	1282
Real	TB2 + HB2 + HB1	2339
DCM8		
Complex	HB3 +HB2 + HB1	1662
Real	HB4 + HB3 + HB2 + HB1	3200
DCM12		
Complex	TB2 + HB2 + HB1	2428
Real	TB2 + HB3 + HB2 + HB1	4540
DCM16		
Complex	HB4 + HB3 + HB2 + HB1	3201
Real	HB5 + HB4 + HB3 + HB2 + HB1	6268
DCM24		
Complex	TB2 + HB3 + HB2 + HB1	4733
Real	TB2 + HB4 + HB3 + HB2 + HB1	8582
DCM32		
Complex	HB5 + HB4 + HB3 + HB2 + HB1	6273
Real	HB6 + HB5 + HB4 + HB3 + HB2 + HB1	12,415
DCM48		
Complex	TB2 + HB4 + HB3 + HB2 + HB1	9337
Real	TB2 + HB5 + HB4 + HB3 + HB2 + HB1	17030

Chip Application Mode	Enabled Filters	ADC + DSP Latency (Clock Cycles)
DCM64		
Complex	HB6 + HB5 + HB4 + HB3 + HB2 + HB1	12416
Real	HB7 + HB6 + HB5 + HB4 + HB3 + HB2 + HB1	24707
DCM96, Complex	TB2 + HB5 + HB4 + HB3 + HB2 + HB1	18552
DCM128, Complex	HB7 + HB6 + HB5 + HB4 + HB3 + HB2 + HB1	24705

[1] DCMx indicates the decimation ratio.

Table 29. Typical Latency Through JESD204B Block (Number of Sample Clocks)[1, 2]

	M/L Ratio[3]							
Chip Application Mode	0.0625	0.125	0.25	0.5	1	2	4	8
Full Bandwidth	187	108	59	N/A	N/A	N/A	N/A	N/A
DCM1, Real	195	112		N/A	N/A	N/A	N/A	N/A
DCM2								
Complex	N/A	236	140	N/A	N/A	N/A	N/A	N/A
Real	396	236	136	N/A	N/A	N/A	N/A	N/A
DCM3, Real	606	347	197	N/A	N/A	N/A	N/A	N/A
DCM4								
Complex	N/A	478	280	150	N/A	N/A	N/A	N/A
Real	810	467	265	130	N/A	N/A	N/A	N/A
DCM6								
Complex	N/A	738	436	246	N/A	N/A	N/A	N/A
Real	1011	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DCM8								
Complex	N/A	830	574	313	182	N/A	N/A	N/A
Real	1281	893		330	190	N/A	N/A	N/A
DCM12								
Complex	N/A	N/A	852	N/A	N/A	N/A	N/A	N/A
Real	N/A	1264	877	N/A	248	N/A	N/A	N/A
DCM16								
Complex	N/A	N/A	1054	689	424	N/A	N/A	N/A
Real	2437	N/A	N/A	614	334	N/A	N/A	N/A
DCM24								
Complex	N/A	2212	N/A	N/A	516	313	N/A	N/A
Real	N/A	2302	1577	1132	725	N/A	N/A	N/A
DCM32								
Complex	N/A	3073	N/A	N/A	850	576	N/A	N/A
Real	N/A	3198	N/A	N/A	803	N/A	N/A	N/A
DCM48								
Complex	N/A	N/A	N/A	1457	773	N/A	N/A	N/A
Real	N/A	N/A	N/A	2066	1361	N/A	N/A	N/A
DCM64								
Complex	N/A	N/A	3988	2306	1685	1123	N/A	N/A
Real	N/A	N/A	N/A	2499	1697	N/A	N/A	N/A
DCM96, Complex	N/A	N/A	5013	2630	1400	798	N/A	N/A
DCM128, Complex	N/A	N/A	N/A	4484	2949	2115	N/A	N/A

[1] N/A means not applicable and indicates that the application mode is not supported at the M/L ratio listed.
[2] High density (HD) bit is set to zero (HD = 0) for all the numbers listed in this table.
[3] M/L ratio is the number of converters divided by the number of lanes for the configuration.

DETERMINISTIC LATENCY

Both ends of the JESD204B link contain various clock domains distributed throughout each system. Data traversing from one clock domain to a different clock domain can lead to ambiguous delays in the JESD204B link. These ambiguities lead to non-repeatable latencies across the link from one power cycle or link reset to the next. Section 6 of the JESD204B specification addresses the issue of deterministic latency with mechanisms defined as Subclass 1 and Subclass 2.

The AD9213 supports JESD204B Subclass 0 and Subclass 1 operation. Register 0x525, Bit 5 sets the subclass mode for the AD9213 and its default is set for Subclass 1 operating mode (Register 0x525, Bit 5 = 1). If deterministic latency is not a system requirement, Subclass 0 operation is recommended and the SYSREF signal may not be required. Even in Subclass 0 mode, the SYSREF signal can required in an application where multiple AD9213 devices must be synchronized with each other.

SUBCLASS 0 OPERATION

If there is no requirement for multi-chip synchronization while operating in subclass 0 mode (Register 0x525, Bit 5 = 0), the SYSREF input can be left disconnected. In this mode, the relationship of the JESD204B clocks between the JESD204B transmitter and receiver are arbitrary but does not affect the ability of the receiver to capture and align the lanes within the link.

SUBCLASS 1 OPERATION

The JESD204B protocol organizes data samples into octets, frames, and multiframes, as described in the Transport Layer section of this data sheet. The LMFC is synchronous with the beginnings of these multiframes. In Subclass 1 operation, the SYSREF_x signal is used to synchronize the LMFCs for each device in a link or across multiple links (within the AD9213, SYSREF_x signal also synchronizes the internal sample dividers). This is illustrated in Figure 122. The JESD204B receiver uses the multiframe boundaries and buffering to achieve consistent latency across lanes (or even multiple devices), and also to achieve a fixed latency between power cycles and link reset conditions.

The AD9213 features both averaged SYSREF and sampled SYSREF modes for JESD204B Subclass 1 operation. Averaged SYSREF mode is valid for all AD9213 sample rates. Sampled SYSREF mode is valid for 2.5 GSPS to 3 GSPS. See the Multichip Synchronization (MCS) section for details.

Deterministic Latency Requirements

Several key factors are required for achieving deterministic latency in a JESD204B Subclass 1 system.

- SYSREF_x signal distribution skew within the system must be less than the desired uncertainty for the system.
- SYSREF_x setup and hold time requirements must be met for each device in the system. With the AD9213 averaged SYSREF mode, there are no setup and hold time requirements for the externally applied SYSREF_x signal. References to SYSREF_x setup and hold times are in the context of the sampled SYSREF mode.
- The total latency variation across all lanes, links and devices must be ≤1 LMFC periods (see Figure 122). This includes both variable delays and the variation in fixed delays from lane to lane, link to link, and device to device in the system.

Setting Deterministic Latency Registers

The JESD204B receive buffer in the logic device buffers data starting on the LMFC boundary. If the total link latency in the system is near an integer multiple of the LMFC period, it is possible that from one power cycle to the next, the data arrival time at the receive buffer can straddle an LMFC boundary. To ensure deterministic latency in this case, a phase adjustment of the LMFC at either the transmitter or receiver will need to be performed. Typically, adjustments to accommodate the receive buffer are made to the LMFC of the receiver. In the AD9213, this adjustment can be made using the LMFC offset register (Register 0x50A, Bits[4:0]). This register delays the LMFC in frame clock increments, depending on the F parameter (number of octets per lane per frame). For F = 1, every fourth setting (0, 4, 8, …) results in a 1-frame clock shift. For F = 2, every other setting (0, 2, 4, …) results in a 1-frame clock shift. For all other values of F, each setting results in a 1-frame clock shift. Figure 123 shows that in the case where the link latency is near an LMFC boundary, the local LMFC of the AD9213 can be delayed to delay the data arrival time at the receiver. Figure 124 shows how the LMFC of the receiver is delayed to accommodate the receive buffer timing. Consult the applicable JESD204B receiver user guide for details on making this adjustment. If the total latency in the system is not near an integer multiple of the LMFC period or if the appropriate adjustments have been made to the LMFC phase at the clock source, it is still possible to have variable latency from one power cycle to the next. In this case, check for the possibility that the setup and hold time requirements for the SYSREF_x signal are not being met. This can be checked by reading the SYSREF setup/hold monitor register (Register 0x1509).

If the read from Register 0x1509 indicates a potential timing problem, the following adjustments can be made. Changing the SYSREF level that is used for alignment is possible using the SYSREF transition select bit (Register 0x1508, Bit 1). Changing which edge of CLK_x is used to capture SYSREF can be done using the CLK edge select bit (Register 0x1508, Bit 0). Both of these options are explained in the Register 0x1508 description in Table 36. If neither of these options achieve an acceptable setup and hold time, adjusting the phase of SYSREF_x and/or the device clock (CLK_x) can be required.

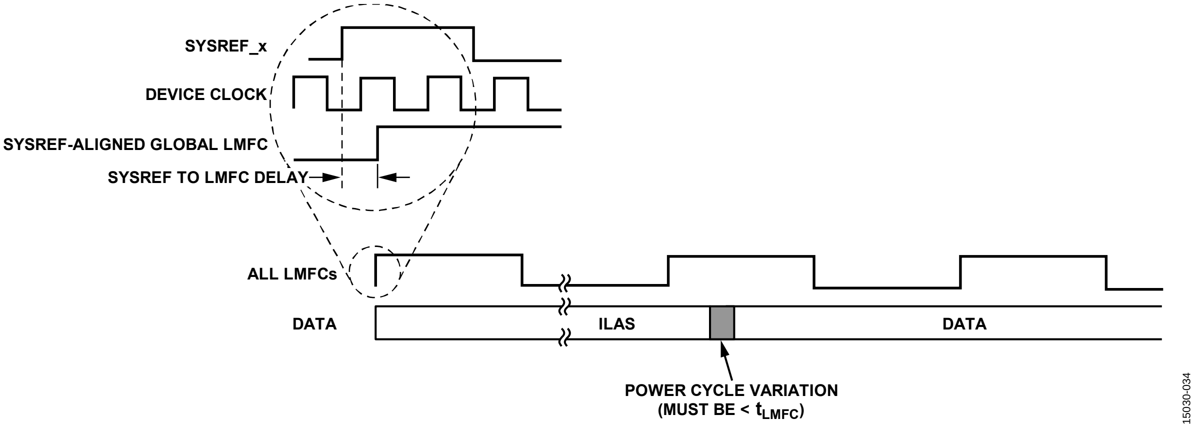


Figure 122. SYSREF_x and LMFC

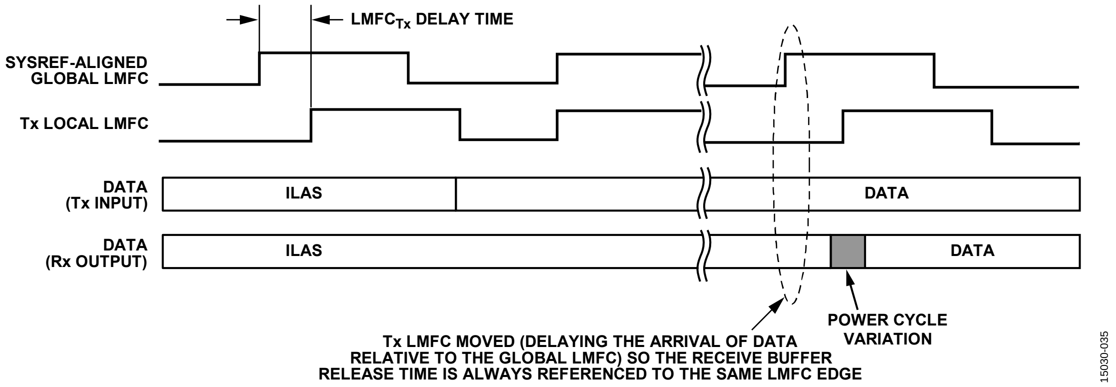


Figure 123. Adjusting the JESD204B Transmitter LMFC in the AD9213

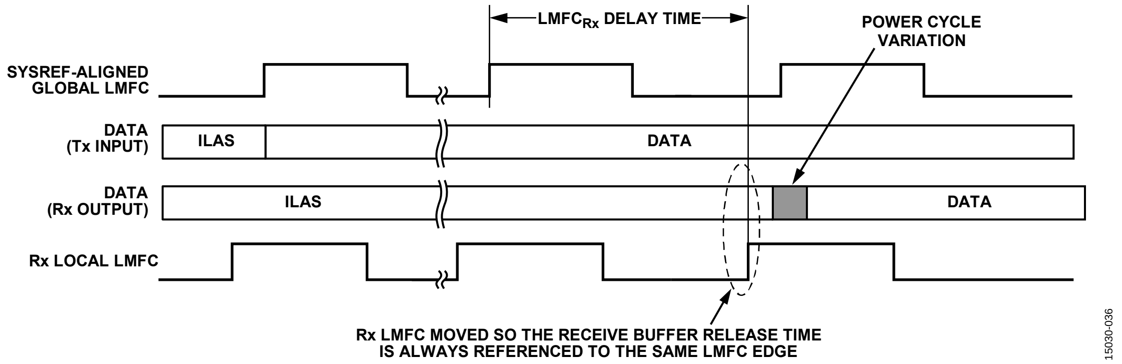


Figure 124. Adjusting the JESD204B Receiver LMFC in the Logic Device

MULTICHIP SYNCHRONIZATION (MCS)

The AD9213 has a JESD204B Subclass 1 compatible SYSREF_x input, which provides flexible options for synchronizing the internal blocks of the AD9213. The SYSREF_x input is a source synchronous system reference signal used to align the AD9213 LMFCs that enables multichip synchronization between multiple AD9213s. The input clock divider, DDC, signal monitor block, and JESD204B link can be synchronized using the SYSREF_x input.

The AD9213 features a mode that averages the applied SYSREF signal to create a stable internal version.

AVERAGED SYSREF MODE FOR MCS

In averaged SYSREF mode, the averaging function determines the phase of the SYSREF_x signal. This information is used to regenerate an internal version, and the averaged version is tolerant to random jitter on external SYSREF_x signal and synchronizes other downstream blocks within the ADC. Multiple AD9213s each use the respective, internally regenerated, averaged, local SYSREF signals.

The following are some characteristics of averaged SYSREF synchronization:

- Uses time to digital converters and filtering to recover phase of the SYSREF signal and create a clean internal local version.
- Assumes the SYSREF signal is continuous or in pulse trains.
- No sampling issues due to setup/hold time violations.
- Timing is recovered from the averaged waveform.
- Extends JESD204B Subclass 1 to the full sample rate of the AD9213.
- Jitter tolerant. Jitter on the SYSREF signal is cleaned up by averaging of SYSREF_x timing.

For the vast majority of sample rates at which the AD9213 is to be used, averaged SYSREF mode is required for JESD204B Subclass 1 operation.

SAMPLED SYSREF MODE

In sampled SYSREF mode, SYSREF_x operates as a standard JESD204B Subclass 1 signal.

The following are some characteristics of sampled SYSREF_x synchronization:

- Synchronous sampling of SYSREF_x.
- Must meet setup/hold time requirements for reliable synchronization. This is increasingly difficult to achieve as the sample rate increases.
- SYSREF_x jitter must be much less than one sample clock period. SYSREF_x coming from ASICs or FPGAs can have significant jitter.

Because the setup and hold time requirements with respect to the sample clock must be met for sampled SYSREF mode to properly synchronize multiple devices, sampled SYSREF mode does not operate properly at the full sample rate of the AD9213.

For multichip synchronization above 3 GSPS, averaged SYSREF mode must be used.

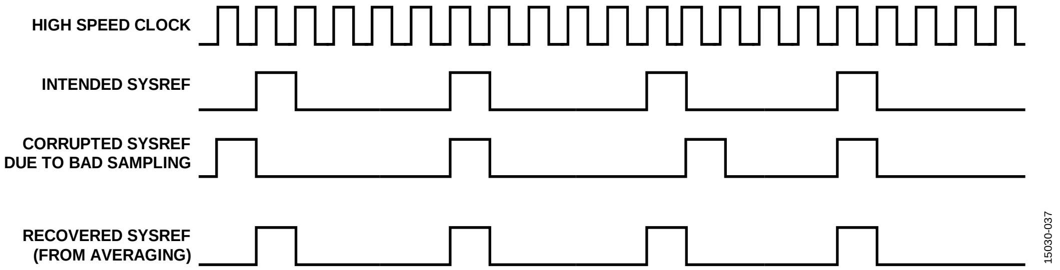


Figure 125. Recovered SYSREF_x

MCS AVERAGED SYSREF MODE SETUP

The following are the SYSREF_x signal constraints for MCS averaged SYSREF mode:

- $(f_{CLK} \div 8) \div (f_{SYSREF\_x})$ must be a positive integer.
- f_{SYSREF_x} must be ≤ 500 MHz
- The number of LMFC cycles (K) per SYSREF_x cycle must be a positive integer.

To calculate LMFC frequency (f_{LMFC}), use the following conditions:

$$f_{LMFC} = f_S/(DCM \times K \times S)$$

$$S = 8 \times F \times L/(N' \times M)$$

$$K = 32 \text{ or } 16 \text{ frames/multiframe}$$

To configure the AD9213 for MCS averaged SYSREF_x mode, take the followings steps:

1. Write Register 0x525, Bit 5 = 1 to select JESD204B Subclass 1 mode. Set the SYSREF_x period. All three of the following registers must be written for the 24-bit KNOWN_SYSREF_PERIOD word (KNOWN_SYSREF_PERIOD[23:0] = $(f_{CLK}/8)/f_{SYSREF\_x}$):
    a. Register 0x1627, Bits[7:0] = KNOWN_SYSREF_PERIOD[7:0]
    b. Register 0x1628, Bits[7:0] = KNOWN_SYSREF_PERIOD[15:8]
    c. Register 0x1629, Bits[7:0] = KNOWN_SYSREF_PERIOD[23:16]

For example, if f_{CLK} = 10 GHz (chosen by user), then,

$S = 8 \times F \times L/(N' \times M) = (8 \times 2 \times 16)/(16 \times 1) = 16$ (calculated automatically within AD9213)

$f_{LFMC} = f_{CLK}/(DCM \times K \times S) = 10 \times 10^{-9}/(1 \times 32 \times 16) =$ 19,531,250 Hz

f_{SYSREF_x} = 4.8828125 MHz, which is chosen for this example to comply with the f_{LFMC} and f_{SYSREF_x} constraint.

With f_{SYSREF_x} in compliance, KNOWN_SYSREF_PERIOD[23:0] can be calculated:

$$KNOWN\_SYSREF\_PERIOD[23:0] =$$

$$\frac{f_{CLK}/8}{f_{SYSREF\_x}} = \frac{10 \times 10^{9}}{4.8828125 \times 10^{6}} = 256 = 0x100$$

The following write operations must be made to set KNOWN_SYSREF_PERIOD[23:0] = 0x100:

- Register 0x1627, Bits[7:0] = 0x00
- Register 0x1628, Bits[7:0] = 0x01
- Register 0x1629, Bits[7:0] = 0x00

2. Set the sample clock period (Register 0x162D to Register 0x1630, Bits[7:0]). Bits[31:16] represent integer values in picoseconds and Bits[15:0] represent fractions of picoseconds.

For example, if f_{CLK} = 6 GHz (chosen by user), then,

Clock period = 1/6 GHz = 166.667 ps

$166.667_{10} = \text{A6.AAC0}_{16}$.

The following writes must be made to set SAMPLE_CLOCK_PERIOD[31:0] = A6.AAC0_{16}:

- Register 0x162D Bits[7:0] = 0xC0
- Register 0x162E Bits[7:0] = 0xAA
- Register 0x162F Bits[7:0] = 0xA6
- Register 0x1630 Bits[7:0] = 0x00

3. Set the number of SYSREF_x pulses to ignore (Register 0x1521, MCS_SYSREF_IGNORE_COUNT[7:0]). Note that this value is system dependent on the number of cycles required to stabilize the SYSREF_x signal. For example, to ignore 100 SYSREF_x pulses, perform the following write operation: Register 0x1521 Bits[7:0] = MCS_SYSREF_IGNORE_COUNT[7:0] = 0x64.
4. Set the SYSREF_x averaging count (Register 0x162A, Bits[7:0] and Register 0x162B, Bits[7:0]). The averaging count is the number of SYSREF_x pulses the MCS uses to determine the timing of the externally applied SYSREF_x signal. The larger the averaging count, the more accurate the result, but it takes longer to achieve MCS lock. Note that the number of SYSREF_x pulses averaged is the (Register contents + 1) × 16. The recommended value for the register contents is ≥1000. For example, to set the averaging count register contents = 1000 = 0x03E8, perform the following write operations: Register 0x162A Bits[7:0] = MCS_SYSREF_AVGING_COUNT[7:0] = 0xE8, and Register 0x162B Bits[7:0] = MCS_SYSREF_AVGING_COUNT[15:8] = 0x03. This example write operation corresponds to averaging (1000 + 1) × 16 ≈ 16,000 SYSREF_x pulses averaged.
5. Select MCS SYSREF averaging mode (Register 0x1621, Bits[3:0]). This action selects averaging mode, which averages the signal present on the analog input of the time to digital converter (TDC) within the MCS block. The instantaneous period is calculated, and this is then averaged to create a clean and stable internal SYSREF_x signal, available for alignment of the LMFC. The following write operation selects SYSREF averaging mode: Register 0x1621, Bits[3:0] = 0x9.
6. Set the MCS phase slip mode (Register 0x1636, Bit 0 = 1). Always set this bit to 1 for SYSREF_x averaging mode.

7. Set to lock once mode. When Register 0x1622, Bits[1:0] = 0x0, the MCS does nothing. When Register 0x1622, Bits[1:0] = 0x2, the MCS locks when it has successfully acquired the averaged SYSREF signal, and remain locked, even if timing conditions change due to temperature. The MCS does not relock in response to changed timing conditions.
8. Set SYSREF_RESYNC. Write Register 0x693 = SYSREF_RESYNC = 0x01. Always set this register to 0x01 for any Subclass 1 operation.
9. Set the USER_CTRL_TRANSFER bit (Register 0x1600, Bit 0 = 1). When set to 1, this bit applies the latest MCS settings. Perform this write every time any of the registers described in this section are changed. This bit is self clearing.
10. Check for SYSREF_x lock in averaging mode after a wait. After the wait interval, check MCS lock by reading Register 0x151E, Bit 1. The wait interval is SYSREF_x averaging count × SYSREF_x period ×100. For example, if the f_{SYSREF_x} = 4.8828125 MHz, the approximate SYSREF_x period is 205 ns. For an averaging count is 16,000, the wait interval is 1000 × 16 × 205 ns × 100 = 328 ms.

If all AD9213 devices intended to be synchronized show MCS lock, the desired result is achieved. Each device has a local SYSREF from which to align the LMFC, which in turn results in deterministic latency. Given enough time, it is highly unlikely that MCS lock is not achieved in lock once mode.

If one or more AD9213s do not achieve MCS lock within the allotted time, the following steps can be taken for all AD9213s to achieve MCS lock:

1. More time can be allotted to achieve MCS lock. In the devices not achieving MCS lock quickly, local SYSREF is by random chance closely aligned with, and slightly ahead of, the applied SYSREF signal, causing a delay in the MCS lock process. This state of the local SYSREF and the applied SYSREF_x being closely aligned is the desired result. However, until the MCS Lock bit goes high, the local SYSREF is not sent to downstream digital circuitry. Longer time taken to achieve MCS lock is not indicative of reduced time alignment accuracy of the local SYSREF.
2. Alternatively, delay can be added to the SYSREF_x path within AD9213 to delay the internal waveform used by the MCS block to create the local SYSREF.
    a. On the devices that have not achieved MCS lock, enable the fine delay cell by setting Register 0x1516, Bit 0 = 1.
    b. Add approximately half of a sample clock cycle delay. Each LSB of Register 0x1517 represents ~1.1 ps delay. For example, half of a 10 GHz clock period is 50 ps. Therefore, set Register 0x1517, Bits[7:0] = 0x2D (45 × 1.1 ps steps = 49.5 ps).
    c. Toggle the transfer bit. Register 0x1600, Bit 0 = 1 to restart the SYSREF_x averaging and MCS lock procedure.
    d. Check for MCS lock, Register 0x151E, Bit 1 = 1.
3. If MCS lock is still not achieved, there are other issues with the setup. Check that the frequency of SYSREF complies with the requirements stated before Step 1. The signal sources of the sample clock and SYSREF must be phase locked. The time difference between the externally applied SYSREF_x signal and the averaged internal version can be monitored by reading the contents of Register 0x1623, Register 0x1624, Register 0x1625, and Register 0x1626. These are four 8-bit registers that comprise a 32-bit word (CALC_TIME_DIFF[31:0]) signifying the calculated time difference between the input SYSREF_x signal and the averaged local SYSREF. Register 0x1623 contains the LSBs and Register 0x1626 contains the MSBs. The TDC is connected to the SYSREF_x input, and the local SYSREF counter. This number is an average of TDC measurements as determined by Register 0x162A and Register 0x162B.

When MCS lock is achieved, the time difference between the externally applied SYSREF signal and the averaged internal version is <1 ADC clock period.

TEST MODES

JESD204B TEST MODES

The AD9213 has flexible test modes in the JESD204B block. These test modes are listed in Register 0x505 and Register 0x506. These test patterns can be injected at various points along the output datapath. These test injection points shown in Figure 115 illustrate the various test modes available in the JESD204B block. For the AD9213, a transition from test modes (Register 0x505 ≠ 0x00) to normal mode (Register 0x505 = 0x00) requires an SPI soft reset. This is done by writing 0x81 to Register 0x0000 (self cleared).

Transport Layer Sample Test Mode

The transport layer samples are implemented in the AD9213 as defined by Section 5.1.6.3 in the JEDEC JESD204B specification. These tests are shown in Register 0x503, Bit 5. The test pattern is equivalent to the raw samples from the ADC.

Interface Test Modes

The interface test modes are described in Register 0x505, Bits[3:0]. These test modes are also explained in Table 31. The interface tests can be injected at various points along the data. See Figure 115 for more information on the test injection points. Register 0x505, Bits[5:4] show where these tests are injected.

Table 32 and Table 33 show examples of some of the test modes when injected at the JESD204B sample input, PHY 10-bit input, and scrambler 8-bit input. UPx in the tables represent the user pattern control bits from the customer register map.

DATA LINK LAYER TEST MODES

The data link layer test modes are implemented in the AD9213 as defined by Section 5.3.3.8.2 in the JEDEC JESD204B specification. These tests are shown in Register 0x506, Bits[2:0]. Test patterns inserted at this point are useful for verifying the functionality of the data link layer. When the data link layer test modes are enabled, disable SYNCINB± by writing 0xC0 to Register 0x504.

Table 30. JESD204B Interface Test Modes

Output Test Mode Bit Sequence	Pattern Name	Expression	Default
0000	Off (default)	Not applicable	Not applicable
0001	Alternating checker board	0x5555, 0xAAAA, 0x5555, …	Not applicable
0010	1/0 word toggle	0x0000, 0xFFFF, 0x0000, …	Not applicable
0011	31-bit PN sequence	$x^{31} + x^{28} + 1$	0x0003AFFF
0100	23-bit PN sequence	$x^{23} + x^{18} + 1$	0x003AFF
0101	15-bit PN sequence	$x^{15} + x^{14} + 1$	0x03AF
0110	9-bit PN sequence	$x^9 + x^5 + 1$	0x092
0111	7-bit PN sequence	$x^7 + x^6 + 1$	0x07
1000	Ramp output	$(x) \% 2^{16}$	Ramp size depends on test injection point
1110	Continuous/repeat user test	Register 0x558 to Register 0x55F	User Pattern 1 to User Pattern 4, then repeat
1111	Single user test	Register 0x558 to Register 0x55F	User Pattern 1 to User Pattern 4, then zeros

Table 31. JESD204B Sample Input for M = 1, S = 16, N' = 16 (Register 0x505, Bits[5:4] = 'b00)

Frame Number	Converter Number	Sample Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0	0	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
		1	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
		2	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
		3	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
		4	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
		5	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
		6	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
		7	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
		8	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
		9	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
		10	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
		11	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
		12	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
		13	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
		14	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
		15	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]

Frame Number	Converter Number	Sample Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
1	0	0	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
		1	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
		2	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
		3	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
		4	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
		5	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
		6	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
		7	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
		8	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
		9	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
		10	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
		11	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
		12	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
		13	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
		14	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
		15	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
2	0	0	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
		1	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
		2	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
		3	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
		4	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
		5	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
		6	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
		7	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
		8	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
		9	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
		10	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
		11	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
		12	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
		13	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
		14	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
		15	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
3	0	0	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
		1	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
		2	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
		3	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
		4	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
		5	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
		6	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
		7	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
		8	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
		9	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
		10	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
		11	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
		12	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
		13	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
		14	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
		15	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
4	0	0	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
	0	1	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
	0	2	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
	0	3	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
	0	4	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
		5	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
		6	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000

Frame Number	Converter Number	Sample Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
		7	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
		8	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
		9	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
		10	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
		11	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
		12	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
		13	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
		14	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
		15	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000

Table 32. Physical Layer 10-Bit Input (Register 0x505, Bits[5:4] = 'b01)

10-Bit Symbol Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0x155	0x000	(x) % 2^{10}	0x125	0x3FD	UP1[15:6]	UP1[15:6]
1	0x2AA	0x3FF	(x + 1) % 2^{10}	0x2FC	0x1C0	UP2[15:6]	UP2[15:6]
2	0x155	0x000	(x + 2) % 2^{10}	0x26A	0x00A	UP3[15:6]	UP3[15:6]
3	0x2AA	0x3FF	(x + 3) % 2^{10}	0x198	0x1B8	UP4[15:6]	UP4[15:6]
4	0x155	0x000	(x + 4) % 2^{10}	0x031	0x028	UP1[15:6]	0x000
5	0x2AA	0x3FF	(x + 5) % 2^{10}	0x251	0x3D7	UP2[15:6]	0x000
6	0x155	0x000	(x + 6) % 2^{10}	0x297	0x0A6	UP3[15:6]	0x000
7	0x2AA	0x3FF	(x + 7) % 2^{10}	0x3D1	0x326	UP4[15:6]	0x000
8	0x155	0x000	(x + 8) % 2^{10}	0x18E	0x10F	UP1[15:6]	0x000
9	0x2AA	0x3FF	(x + 9) % 2^{10}	0x2CB	0x3FD	UP2[15:6]	0x000
10	0x155	0x000	(x + 10) % 2^{10}	0x0F1	0x31E	UP3[15:6]	0x000
11	0x2AA	0x3FF	(x + 11) % 2^{10}	0x3DD	0x008	UP4[15:6]	0x000

Table 33. Scrambler 8-Bit Input (Register 0x505, Bits[5:4] = 'b10)

8-Bit Octet Number	Alternating Checkerboard	1/0 Word Toggle	Ramp[1]	PN9	PN23	User Repeat	User Single
0	0x55	0x00	(x) % 2^{8}	0x49	0xFF	UP1[15:9]	UP1[15:9]
1	0xAA	0xFF	(x + 1) % 2^{8}	0x6F	0x5C	UP2[15:9]	UP2[15:9]
2	0x55	0x00	(x + 2) % 2^{8}	0xC9	0x00	UP3[15:9]	UP3[15:9]
3	0xAA	0xFF	(x + 3) % 2^{8}	0xA9	0x29	UP4[15:9]	UP4[15:9]
4	0x55	0x00	(x + 4) % 2^{8}	0x98	0xB8	UP1[15:9]	0x00
5	0xAA	0xFF	(x + 5) % 2^{8}	0x0C	0x0A	UP2[15:9]	0x00
6	0x55	0x00	(x + 6) % 2^{8}	0x65	0x3D	UP3[15:9]	0x00
7	0xAA	0xFF	(x + 7) % 2^{8}	0x1A	0x72	UP4[15:9]	0x00
8	0x55	0x00	(x + 8) % 2^{8}	0x5F	0x9B	UP1[15:9]	0x00
9	0xAA	0xFF	(x + 9) % 2^{8}	0xD1	0x26	UP2[15:9]	0x00
10	0x55	0x00	(x + 10) % 2^{8}	0x63	0x43	UP3[15:9]	0x00
11	0xAA	0xFF	(x + 11) % 2^{8}	0xAC	0xFF	UP4[15:9]	0x00

SERIAL PORT INTERFACE (SPI)

The AD9213 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the Serial Control Interface Standard (Rev. 1.0).

CONFIGURATION USING THE SPI

Three pins define the SPI of the AD9213 ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 34). The SCLK (serial clock) pin is used to synchronize the read and write data presented to and from the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found Figure 3 and Table 5.

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device. This process is called streaming. The CSB can stall high between bytes to allow additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued, which allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the Serial Control Interface Standard (Rev. 1.0).

SPI ACCESSIBLE FEATURES

Table 35 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the Serial Control Interface Standard (Rev. 1.0). The AD9213 device specific features are described in the Memory Map section.

HARDWARE INTERFACE

The pins described in Table 34 comprise the physical interface between the user programming device and the serial port of the AD9213. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9213 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

Table 34. SPI Pins

Pin Name	Function
SCLK	Serial clock. The serial shift clock input that is used to synchronize serial interface, reads, and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles.

Table 35. SPI Accessible Features

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode.
Clock	Allows the user to access the clock frequency change registers SPI.
DDC	Allows the user to set up decimation filters for different applications.
Test Input/Output	Allows the user to set test modes to have known data on output bits.
Output Mode	Allows the user to set up outputs.
SERDES Output Setup	Allows the user to vary SERDES settings such as swing and emphasis.

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLES

Table 36 documents the default hexadecimal value for each hexadecimal address shown. All address locations that are not included in Table 36 are not currently supported for this device and should not be written.

Open and Reserved Locations

All address and bit locations that are not included in Table 36 are not currently supported for this device. Write unused bits of a valid address location with 0s unless the default value is set otherwise. Writing to these locations is required only when part of an address location is unassigned. If the entire address location is open, do not write to this address location.

Default Values

After the AD9213 is reset, critical registers are loaded with default values. The default values for the registers are given in Table 36.

Logic Levels

An explanation of logic level terminology follows:

- Bit is set is synonymous with bit is set to Logic 1 or writing Logic 1 for the bit.
- Clear a bit is synonymous with bit is set to Logic 0 or writing Logic 0 for the bit.
- X denotes a don't care bit.

SPI Soft Reset

After issuing a soft reset by programming Register 0x000, the AD9213 requires 300 ms to recover. When programming the AD9213 for application setup, ensure that an adequate delay is programmed into the firmware after asserting the soft reset and before starting the device setup.

Table 36. Register Map

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x0	SPI_CONFIG_A	7	SOFT_RESET_1		Initiates a Reset Equivalent to a Hard Reset.	0x0	R/W
				0	Do nothing.		
				1	Reset the SPI and registers (self clearing).		
		6	LSB_FIRST_1		LSB/MSB Bit Shift First.	0x0	R/W
				0	Most significant bit shifted first.		
				1	Least significant bit shifted first.		
		5	ADDR_ASCENSION_1		Multibyte SPI Operations Address Increment.	0x1	R/W
				0	Autodecrement.		
				1	Autoincrement.		
		[4:3]	Reserved		Reserved.	0x0	R
		2	ADDR_ASCENSION_0		Multibyte SPI Operations Address Increment.	0x1	R/W
				0	Autodecrement.		
				1	Autoincrement.		
		1	LSB_FIRST_0		LSB/MSB Bit Shift First.	0x0	R/W
				0	Most significant bit shifted first.		
				1	Least significant bit shifted first.		
		0	SOFT_RESET_0		Initiates a Reset Equivalent to a Hard Reset.	0x0	R/W
				0	Do nothing.		
				1	Reset the SPI and registers (self clearing).		
0x2	DEVICE_CONFIG	[7:2]	Reserved		Reserved.	0x3C	R
		[1:0]	OP_MODE		Operating Mode.	0x0	R/W
				00	Normal operation.		
				10	Standby mode.		
				11	Power-down mode.		
0x3	CHIP_TYPE	[7:0]	CHIP_TYPE		High Speed ADCs.	0x3	R
0x4	CHIP_ID_LSB	[7:0]	CHIP_ID[7:0]		Chip ID.	0xE5	R
0x5	CHIP_ID_MSB	[7:0]	CHIP_ID[15:8]		Chip ID.	0x0	R
0xA	CHIP_SCRATCH	[7:0]	CHIP_SCRATCH		Chip Scratch Pad Register.	0x0	R/W
0xC	VENDOR_ID_LSB	[7:0]	CHIP_VENDOR_ID[7:0]		Vendor ID.	0x56	R
0xD	VENDOR_ID_MSB	[7:0]	CHIP_VENDOR_ID[15:8]		Vendor ID.	0x4	R
0x26	GEN_CTRL	[7:4]	Reserved		Reserved.	0x0	R
		3	CLK_SWITCH		Clock Ready (Self Clearing).	0x0	R/W
		[2:0]	Reserved		Reserved.	0x0	R

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x100	FD_CTRL	[7:3]	Reserved		Reserved.	0x0	R
		2	FD_FINE_EN		Enable Fast Detect on Corrected ADC Data.	0x0	R/W
				0	Fast detect disabled.		
				1	Fast detect enabled.		
		1	FD_FORCE_VAL		Force Value for the Fast Detect. This bit field value is forced on the FD pin when FD_FORCE is high.	0x0	R/W
		0	FD_FORCE		Force the Fast Detect Output Pin.	0x0	R/W
				0	Normal operation of the FD pin.		
				1	Force a value on the FD pin (see Bit 1).		
0x101	FD_UP_THRESH_LSB	[7:0]	FD_UP_THRESH[7:0]		Fast Detect Upper Threshold Unsigned Number. 11-bit value for the fast detect upper threshold. The fast detect goes high if the analog input is above the upper threshold value for one f_S/16 clock cycle.	0x0	R/W
0x102	FD_UP_THRESH_MSB	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	FD_UP_THRESH[10:8]		Fast Detect Upper Threshold Unsigned Number. 11-bit value for the fast detect upper threshold. The fast detect goes high if the analog input is above the upper threshold value for one f_S/16 clock cycle.	0x0	R/W
0x103	FD_LOW_THRESH_LSB	[7:0]	FD_LOW_THRESH[7:0]		Fast Detect Lower Threshold Unsigned Number. 11-bit value for the fast detect lower threshold. The fast detect goes low if the analog input is below the lower threshold value for DWELL_THRESH time.	0x0	R/W
0x104	FD_LOW_THRESH_MSB	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	FD_LOW_THRESH[10:8]		Fast Detect Lower Threshold Unsigned Number. 11-bit value for the fast detect lower threshold. The fast detect goes low if the analog input is below the lower threshold value for DWELL_THRESH time.	0x0	R/W
0x105	FD_DWELL_THRESH_LSB	[7:0]	FD_DWELL_THRESH[7:0]		Fast Detect Dwell Time Counter Target. The fast detect goes low if the analog input is below the fast detect lower threshold value for the FD_DWELL_THRESH time. This is a 16-bit counter. Value is in multiples of 16.	0x0	R/W
0x106	FD_DWELL_THRESH_MSB	[7:0]	FD_DWELL_THRESH[15:8]		Fast Detect Dwell Time Counter Target. The fast detect goes low if the analog input is below the fast detect lower threshold value for the FD_DWELL_THRESH time. This is a 16-bit counter. Value is in multiples of 16.	0x0	R/W
0x120	SMON_STATUS_0	[7:0]	SMON_STATUS[7:0]		20-bit Signal Monitor Serial Data Output Bits. Signal monitor data output status bits. Bits[19:9] contain the peak magnitude value obtained over the programmable SMON_PERIOD.	0x0	R
0x121	SMON_STATUS_1	[7:0]	SMON_STATUS[15:8]		20-bit Signal Monitor Serial Data Output Bits. Signal monitor data output status bits. Bits[19:9] contain the peak magnitude value obtained over the programmable SMON_PERIOD.	0x0	R
0x122	SMON_STATUS_2	[7:0]	SMON_STATUS[19:16]		20-bit Signal Monitor Serial Data Output Bits. Signal monitor data output status bits. Bits[19:9] contain the peak magnitude value obtained over the programmable SMON_PERIOD.	0x0	R
0x123	SMON_STATUS_FCNT	[7:0]	SMON_STATUS_FCNT		Signal Monitor Frame Counter. Increments whenever period counter expires. The counter value can be read back from this bit field whenever the SMON_STATUS_UPDATE signal is pulled high.	0x0	R
0x124	SMON_PERIOD_0	[7:0]	SMON_PERIOD[7:0]		2-Bit Value, Sets Number of Clock Cycles that Signal Monitor Performs Operation. 24-bit period value over which the signal monitor performs the peak detection. The bit value must be in multiples of 16.	0x0	R/W

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x125	SMON_PERIOD_1	[7:0]	SMON_PERIOD[15:8]		2-Bit Value, Sets Number of Clock Cycles that Signal Monitor Performs Operation. 24-bit period value over which the signal monitor performs the peak detection. The bit value must be in multiples of 16.	0x0	R/W
0x126	SMON_PERIOD_2	[7:0]	SMON_PERIOD[23:16]		2-Bit Value, Sets Number of Clock Cycles that Signal Monitor Performs Operation. 24-bit period value over which the signal monitor performs the peak detection. The bit value must be in multiples of 16.	0x0	R/W
0x127	SMON_STATUS_CTRL	[7:5]	Reserved		Reserved.	0x0	R
		4	SMON_PEAK_EN		Signal Monitor Peak Detector Enable.	0x0	R/W
				0	Disabled.		
				1	Enabled.		
		[3:1]	SMON_STATUS_RDSEL		Signal Monitor Status Readback Selection. 0x1 for peak detector.	0x0	R/W
				1	Peak detector data.		
		0	SMON_STATUS_UPDATE		A high transition on this signal causes the status value to change in the register map. When this bit field is pulled high, the SMON_STATUS updates with the next value of the peak magnitude.	0x0	R/W
0x128	SMON_SFRAMER	[7:2]	SMON_SFRAMER_INSEL		Signal Monitor Serial Framer Input Selection.	0x0	R/W
				2	Peak magnitude is sent through the frame.		
		1	SMON_SFRAMER_MODE		Signal Monitor Serial Framer Mode Selection.	0x0	R/W
				1	5-bit framer selection.		
		0	SMON_SFRAMER_EN		Signal Monitor Serial Framer Enable.	0x0	R/W
				0	Disabled.		
				1	Enabled.		
0x129	SMON_SYNC_CTRL	[7:2]	Reserved		Reserved.	0x0	R
		1	SMON_SYNC_NEXT		SMON Next Synchronization Mode.	0x0	R/W
				0	Continuous mode.		
				1	Next synchronization mode. In this mode, only the next valid edge of SYSREF_x pin synchronizes the SMON block. Subsequent edges of the SYSREF_x pin are ignored. The SMON_SYNC_EN bit clears when the next SYSREF_x edge is found.		
		0	SMON_SYNC_EN		SMON Synchronization Enable.	0x0	R/W
				0	Disabled.		
				1	Enabled. When synchronization is enabled, if SMON_SYNC_NEXT = 1, only the next valid edge of the SYSREF_x pin synchronizes the SMON block. Subsequent edges of the SYSREF_x pin are ignored. This bit clears when the next SYSREF_x edge is received.		
0x131	SMON_CLK_EN	[7:1]	RESERVED		Reserved.	0x0	R
		0	SMON_CLK_EN		SMON Output Clock Enable.	0x0	R/W
				0	Disabled.		
				1	Enabled.		
0x332	CLK_CHG_REQ	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	CLKCHGREQ		Request Sample Clock Frequency Change.	0x0	R/W
0x500	PLL_CTRL	7	JTX_PLL_BYPASS_LOCK		Bypass PLL Lock Input.	0x0	R/W
		[6:4]	Reserved		Reserved.	0x0	R
		[3:0]	JTX_LOW_LINE_RATE		JESD Low Line Rate Selection.	0x0	R/W
				0011	Lane rate = 13.6 Gbps to 16 Gbps.		
				0000	Lane rate = 6.8 Gbps to 13.6 Gbps.		
				0001	Lane rate = 3.4 Gbps to 6.8 Gbps.		
				0101	Lane rate = 1.7 Gbps to 3.4 Gbps.		

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x501	PLL_STATUS	7	JTX_PLL_LOCKED		PLL Locked Status Bit	0x1	R
				0	Not Locked.		
				1	Locked.		
		[6:0]	Reserved		Reserved.	0x0	R
0x503	JTX_LINK_CTRL1	7	JTX_LINK_STDBY_MODE		JESD204B Standby Mode.	0x0	R/W
				0	Standby mode forces zeros for all converter samples.		
				1	Standby mode forces code group synchronization, /K28.5/characters.		
		6	JTX_TAIL_PN_EN		JESD204B Serial Tail Bit Pseudo Random Number (PN) Enable.	0x0	R/W
				0	Disable.		
				1	Enable.		
		5	JTX_TEST_SAMPLE_EN		JESD204B Serial Test Sample Enable.	0x0	R/W
				0	JESD204B test samples disabled.		
				1	JESD204B test samples enabled. Long transport layer test sample sequence sent on all link lanes (as specified in JESD204B Section 5.1.6.3).		
		4	JTX_LSYNC_EN		JESD204B Serial Lane Synchronization Enable.	0x1	R/W
				0	Disable FACI uses /K28.7/.		
				1	Enable FACI uses /K28.3/ and /K28.7/.		
		[3:2]	JTX_ILAS_MODE		JESD204B Serial Initial Lane Alignment Sequence Mode.	0x1	R/W
				0	Initial lane alignment sequence disabled (JESD204B Section 5.3.3.5).		
				1	Initial lane alignment sequence enabled (JESD204B Section 5.3.3.5).		
				11	Initial lane alignment sequence always in test mode. JESD204B data link layer test mode sent on all lanes where lane alignment sequence repeats as specified in JESD204B Section 5.3.3.8.s.		
		1	JTX_FACI_DISABLE		JESD204B Serial Frame Alignment Character Insertion (FACI) Disable.	0x0	R/W
				0	Frame alignment character insertion enabled (JESD204B Section 5.3.3.4).		
				1	Frame alignment character insertion disabled. For debug only (JESD204B Section 5.3.3.4).		
		0	JTX_LINK_PD		JESD204B Serial Transmit Link Power Down (Active High).	0x0	R/W
				0	JESD204B serial transmit link enabled. Transmission of the /K28.5/ characters for code group synchronization is controlled by the SYNCINB_x pins.		
				1	JESD204B serial transmit link powered down (held in reset and clock gated).		
0x504	JTX_LINK_CTRL2	[7:6]	JTX_SYNC_PIN_MODE		JESD204B Serial Synchronization Mode.	0x0	R/W
				0	Normal mode.		
				10	Ignore SYNCINB_x (force CGS).		
				11	Ignore SYNCINB_x (force ILAS/user data).		
		5	JTX_SYNC_PIN_INV		JESD204B Serial Synchronization Pin Invert.	0x0	R/W
				0	SYNCINB_x pin invert. SYNCINB_x pin not inverted.		
				1	SYNCINB_x pin invert. SYNCINB_x pin inverted.		

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
		4	JTX_SYNC_PIN_TYPE		JESD204B Serial SYNCINB_x Logic Type.	0x1	R/W
				0	SYNCINB_x pin type. CMOS, single-ended SYNCINB_x input. SYNCINB_P used. Requires user to set Register 0x508, Bit 5.		
				1	SYNCINB_x pin type. LVDS differential pair SYNCINB_x input. Requires 100 Ω, external differential termination.		
		3	Reserved		Reserved.	0x0	R
		2	JTX_8B10B_BYPASS		JESD204B Serial 8-Bit/10-Bit Bypass (Test Mode Only).	0x0	R/W
				0	8-bit/10-bit enabled.		
				1	8-bit/10-bit bypassed (two most significant bits are 0).		
		1	JTX_10B_INV		JESD204B 10b Serial Transmit Bit Invert.	0x0	R/W
				0	Normal.		
				1	Invert a, b, c, d, e, f, g, h, i, and j symbols.		
		0	JTX_10B_MIRROR		JESD204B 10-Bit Serial Transmit Bit Mirror.	0x0	R/W
0x505	JTX_LINK_CTRL3	[7:6]	JTX_CHKSUM_MODE		JESD204B Checksum Mode.	0x0	R/W
				00	Checksum is the sum of all 8-bit registers in the link configuration table.		
				01	Checksum is the sum of all individual link configuration fields (LSB aligned).		
				10	Checksum is disabled (set to zero). For test purposes only.		
				11	Unused.		
		[5:4]	JTX_TEST_GEN_SEL		JESD204B Serial Test Generation Input Selection.	0x0	R/W
				00	N' sample input.		
				01	10-bit data at 8-bit/10-bit output (for PHY testing).		
				10	8-bit data at scrambler input.		
		[3:0]	JTX_TEST_GEN_MODE		JESD204B Serial Test Generation Mode.	0x0	R/W
				0000	Normal operation (test mode disabled).		
				0001	Alternating checker board.		
				0010	1/0 word toggle.		
				0011	31-bit PN sequence: $x^{31} + x^{28} + 1$.		
				0100	23-bit PN sequence: $x^{23} + x^{18} + 1$.		
				0101	15-bit PN sequence: $x^{15} + x^{14} + 1$.		
				0110	9-bit PN sequence: $x^{9} + x^{5} + 1$.		
				0111	7-bit sequence: $x^{7} + x^{6} + 1$.		
				1000	Ramp output.		
				1110	Continuous/repeat user test.		
				1111	Single use test.		
0x506	JTX_LINK_CTRL4	[7:4]	JTX_ILAS_DELAY		Initial Lane Alignment Delay.	0x0	R/W
				0000	Transmit ILAS on first LMFC after SYNCINB_x is deasserted.		
				0001	Transmit ILAS on second LMFC after SYNCINB_x is deasserted.		
				0010	Transmit ILAS on third LMFC after SYNCINB_x is deasserted.		
				0011	Transmit ILAS on fourth LMFC after SYNCINB_x is deasserted.		
				0100	Transmit ILAS on fifth LMFC after SYNCINB_x is deasserted.		
				0101	Transmit ILAS on sixth LMFC after SYNCINB_x is deasserted.		
				0110	Transmit ILAS on seven LMFC after SYNCINB_x is deasserted.		
				0111	Transmit ILAS on eighth LMFC after SYNCINB_x is deasserted.		
				1000	Transmit ILAS on ninth LMFC after SYNCINB_x is deasserted.		

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
				1001	Transmit ILAS on tenth LMFC after SYNCINB_x is deasserted.		
				1010	Transmit ILAS on eleventh LMFC after SYNCINB_x is deasserted.		
				1011	Transmit ILAS on twelfth LMFC after SYNCINB_x is deasserted.		
				1100	Transmit ILAS on thirteenth LMFC after SYNCINB_x is deasserted.		
				1101	Transmit ILAS on fourteenth LMFC after SYNCINB_x is deasserted.		
				1110	Transmit ILAS on fifteenth LMFC after SYNCINB_x is deasserted.		
				1111	Transmit ILAS on sixteenth LMFC after SYNCINB_x is deasserted.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	JTX_TEST_LINK_MODE		Link Layer Test Modes.	0x0	R/W
				000	Normal operation (link layer test mode disabled).		
				001	Continuous sequence of /D21.5/ characters.		
				010	Reserved.		
				011	Reserved.		
				100	Modified random pattern (RPAT) test sequence.		
				101	Jitter scrambled pattern (JSPAT) test sequence.		
				110	Jitter tolerance scrambled pattern (JTSPAT) test sequence.		
				111	Reserved.		
0x507	JTX_LINK_CTRL5	[7:0]	JTX_ILAS_CNT		Initial Lane Alignment Sequence Count.	0x0	R/W
0x508	JTX_SYNC_CTRL	[7:6]	Reserved		Reserved.	0x0	R
		5	SPI_CMOS_EN_RC		SYNCINB_x Pin CMOS Enable.	0x0	R/W
				0	CMOS synchronization buffer off.		
				1	CMOS synchronization buffer on.		
		[4:0]	Reserved		Reserved.	0x0	R/W
0x509	JTX_CS_BITS_CTRL	[7:2]	Reserved		Reserved.	0x0	R
		[1:0]	JTX_CS_BITS_MODE		Determines Source of Data Contained in JESD204B Control Bits.	0x2	R/W
				0x0	Disabled.		
				0x1	DFORMAT output (Register 0x620 and Register 0x621).		
				0x2	Undefined.		
				0x3	Undefined.		
0x50A	JTX_LMFC_OFFSET	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LMFC_OFFSET		LMFC Phase Offset Value. Refer to the Deterministic Latency section.	0x0	R/W
0x50E	JTX_DID_CFG	[7:0]	JTX_DID_CFG		JESD204B Serial Device Identification (DID) Number.	0x0	R/W
0x50F	JTX_BID_CFG	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	JTX_BID_CFG		JESD204B Serial Bank Identification (BID) Number (extension to DID).	0x0	R/W
0x510	JTX_LID0_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LID0_CFG		JESD204B Serial Lane Identification (LID) Number for Lane 0.	0x0	R/W
0x511	JTX_LID1_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LID1_CFG		JESD204B Serial LID Number for Lane 1.	0x1	R/W
0x512	JTX_LID2_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LID2_CFG		JESD204B Serial LID Number for Lane 2.	0x2	R/W
0x513	JTX_LID3_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LID3_CFG		JESD204B Serial LID Number for Lane 3.	0x3	R/W
0x514	JTX_LID4_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LID4_CFG		JESD204B Serial LID Number for Lane 4.	0x4	R/W

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x515	JTX_LID5_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LID5_CFG		JESD204B Serial LID Number for Lane 5.	0x5	R/W
0x516	JTX_LID6_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LID6_CFG		JESD204B Serial LID Number for Lane 6.	0x6	R/W
0x517	JTX_LID7_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LID7_CFG		JESD204B Serial LID Number for Lane 7.	0x7	R/W
0x518	JTX_LID8_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LID8_CFG		JESD204B Serial LID Number for Lane 8.	0x8	R/W
0x519	JTX_LID9_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LID9_CFG		JESD204B Serial LID Number for Lane 9.	0x9	R/W
0x51A	JTX_LID10_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LID10_CFG		JESD204B Serial LID Number for Lane 10.	0xA	R/W
0x51B	JTX_LID11_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LID11_CFG		JESD204B Serial LID Number for Lane 11.	0xB	R/W
0x51C	JTX_LID12_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LID12_CFG		JESD204B Serial LID Number for Lane 12.	0xC	R/W
0x51D	JTX_LID13_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LID13_CFG		JESD204B Serial LID Number for Lane 13.	0xD	R/W
0x51E	JTX_LID14_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LID14_CFG		JESD204B Serial LID Number for Lane 14.	0xE	R/W
0x51F	JTX_LID15_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_LID15_CFG		JESD204B Serial LID Number for Lane 15.	0xF	R/W
0x520	JTX_SCR_L_CFG	7	JTX_SCR_CFG		JESD204B Serial Scrambler Mode (SCR = JTX_SCR_CFG).	0x1	R/W
				0	JESD204B scrambler disabled (SCR = 0).		
				1	JESD204B scrambler enabled (SCR = 1).		
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_L_CFG		JESD204B Serial Lane Control (L = JTX_L_CFG + 1).	0xF	R/W
				0x0	One lane per link (L = 1).		
				0x1	Two lanes per link (L = 2).		
				0x2	Three lanes per link (L = 3).		
				0x3	Four lanes per link (L = 4).		
				0x5	Six lanes per link (L = 6).		
				0x7	Eight lanes per link (L = 8).		
				0xB	Twelve lanes per link (L = 12).		
				0xF	Sixteen lanes per link (L = 16).		
0x521	JTX_F_CFG	[7:0]	JTX_F_CFG		JESD204B Number of Octets per Frame (F = JTX_F_CFG + 1).	0x1	R/W
				0000	F = 1.		
				0001	F = 2.		
				0011	F = 4.		
0x522	JTX_K_CFG	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_K_CFG		JESD204B Number of Frames per Multiframe (K = JTX_K_CFG + 1).	0x1F	R/W
0x523	JTX_M_CFG	[7:0]	JTX_M_CFG		JESD204B Number of Converters per Link (M = JTX_M_CFG).	0x0	R/W
				000	Link connected to one virtual converter (M = 1).		
				001	Link connected to two virtual converters (M = 2).		
0x524	JTX_CS_N_CFG	[7:6]	JTX_CS_CFG		JESD204B Number of Control bits per Sample.	0x3	R/W
				00	No control bits (CS = 0).		
				01	One control bit (CS = 1), Control Bit 2 only.		
				10	Two control bits (CS = 2), Control Bit 2 and Control Bit 1 only.		
				11	Three control bits (CS = 3), all control bits (Control Bit 2, Control Bit 1, and Control Bit 0).		
		5	Reserved		Reserved.	0x0	R

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
		[4:0]	JTX_N_CFG		JESD204B Converter Resolution (N = JTX_N_CFG + 1).	0x0B	R/W
				00110	N = 7-bit resolution.		
				00111	N = 8-bit resolution.		
				01000	N = 9-bit resolution.		
				01001	N = 10-bit resolution.		
				01010	N = 11-bit resolution.		
				01011	N = 12-bit resolution.		
				01100	N = 13-bit resolution.		
				01101	N = 14-bit resolution.		
				01110	N = 15-bit resolution.		
				01111	N = 16-bit resolution.		
0x525	JTX_SCV_NP_CFG	[7:5]	JTX_SUBCLASSV_CFG		JESD204B Device Subclass Version.	0x1	R/W
				000	Subclass 0.		
				001	Subclass 1.		
		[4:0]	JTX_NP_CFG		JESD204B Total Number of Bits per Sample (N' = JTX_NP_CFG + 1).	0xF	R/W
				00111	N' = 8.		
				01011	N' = 12.		
				01111	N' = 16.		
0x526	JTX_JV_S_CFG	[7:5]	Reserved		Reserved.	0x1	R
		[4:0]	JTX_S_CFG		JESD204B Samples Per Converter Frame Cycle (S = JTX_S_CFG + 1).	0xF	R
0x527	JTX_HD_CF_CFG	7	JTX_HD_CFG		JESD204B High Density Format (HD).	0x0	R
				0	High density format disabled.		
				1	High density format enabled.		
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	JTX_CF_CFG		JESD204B Number of Control Words per Frame Clock Cycle per Link (CF = JTX_CF_CFG).	0x0	R
0x52B	JTX_CHKSUM0_CFG	[7:0]	JTX_CHKSUM0_CFG		JESD204B Serial Checksum Value of Lane 0. Serial checksum value for Lane 0. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 0) mod 256.	0xDC	R
0x52C	JTX_CHKSUM1_CFG	[7:0]	JTX_CHKSUM1_CFG		JESD204B Serial Checksum Value of Lane 1. Serial checksum value for Lane 1. Automatically calculated for each lane. Sum (all link configuration parameter for Lane 1) mod 256.	0xDD	R
0x52D	JTX_CHKSUM2_CFG	[7:0]	JTX_CHKSUM2_CFG		JESD204B Serial Checksum Value of Lane 2. Serial checksum value for Lane 2. Automatically calculated for each lane. Sum (all link configuration parameter for Lane 2) mod 256.	0xC5	R
0x52E	JTX_CHKSUM3_CFG	[7:0]	JTX_CHKSUM3_CFG		JESD204B Serial Checksum Value of Lane 3. Serial checksum value for Lane 3. Automatically calculated for each lane. Sum (all link configuration parameter for Lane 3) mod 256.	0xDF	R
0x52F	JTX_CHKSUM4_CFG	[7:0]	JTX_CHKSUM4_CFG		JESD204B Serial Checksum Value of Lane 4. Serial checksum value for Lane 4. Automatically calculated for each lane. Sum (all link configuration parameter for Lane 4) mod 256.	0xE0	R
0x530	JTX_CHKSUM5_CFG	[7:0]	JTX_CHKSUM5_CFG		JESD204B Serial Checksum Value of Lane 5. Serial checksum value for Lane 5. Automatically calculated for each lane. Sum (all link configuration parameter for Lane 5) mod 256.	0xE1	R
0x531	JTX_CHKSUM6_CFG	[7:0]	JTX_CHKSUM6_CFG		JESD204B Serial Checksum Value of Lane 6. Serial checksum value for Lane 6. Automatically calculated for each lane. Sum (all link configuration parameter for Lane 6) mod 256.	0xE2	R
0x532	JTX_CHKSUM7_CFG	[7:0]	JTX_CHKSUM7_CFG		JESD204B Serial Checksum Value of Lane 7. Serial checksum value for Lane 7. Automatically calculated for each lane. Sum (all link configuration parameter for Lane 7) mod 256.	0xE3	R

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x533	JTX_CHKSUM8_CFG	[7:0]	JTX_CHKSUM8_CFG		JESD204B Serial Checksum Value of Lane 8. Serial checksum value for Lane 8. Automatically calculated for each lane. Sum (all link configuration parameter for Lane 8) mod 256.	0xE4	R
0x534	JTX_CHKSUM9_CFG	[7:0]	JTX_CHKSUM9_CFG		JESD204B Serial Checksum Value of Lane 9. Serial checksum value for Lane 9. Automatically calculated for each lane. Sum (all link configuration parameter for Lane 9) mod 256.	0xE5	R
0x535	JTX_CHKSUM10_CFG	[7:0]	JTX_CHKSUM10_CFG		JESD204B Serial Checksum Value of Lane 10. Serial checksum value for Lane 10. Automatically calculated for each lane. Sum (all link configuration parameter for Lane 10) mod 256.	0xE6	R
0x536	JTX_CHKSUM11_CFG	[7:0]	JTX_CHKSUM11_CFG		JESD204B Serial Checksum Value of Lane 11. Serial checksum value for Lane 11. Automatically calculated for each lane. Sum (all link configuration parameter for Lane 11) mod 256.	0xE7	R
0x537	JTX_CHKSUM12_CFG	[7:0]	JTX_CHKSUM12_CFG		JESD204B Serial Checksum Value of Lane 12. Serial checksum value for Lane 12. Automatically calculated for each lane. Sum (all link configuration parameter for Lane 12) mod 256.	0xE8	R
0x538	JTX_CHKSUM13_CFG	[7:0]	JTX_CHKSUM13_CFG		JESD204B Serial Checksum Value of Lane 13. Serial checksum value for Lane 13. Automatically calculated for each lane. Sum (all link configuration parameter for Lane 13) mod 256.	0xE9	R
0x539	JTX_CHKSUM14_CFG	[7:0]	JTX_CHKSUM14_CFG		JESD204B Serial Checksum Value of Lane 14. Serial checksum value for Lane 14. Automatically calculated for each lane. Sum (all link configuration parameter for Lane 14) mod 256.	0xEA	R
0x53A	JTX_CHKSUM15_CFG	[7:0]	JTX_CHKSUM15_CFG		JESD204B Serial Checksum Value of Lane 15. Serial checksum value for Lane 15. Automatically calculated for each lane. Sum (all link configuration parameter for Lane 15) mod 256.	0xEB	R
0x53B	JTX_LANE_PDWN	[7:0]	JTX_FORCE_LANE_PD[7:0]		Physical Lane Force Power-Down. 16-bit bit fields are split into two registers. JTX_FORCE_LANE_PD[7] = Lane 7 force power-down. JTX_FORCE_LANE_PD[6] = Lane 6 force power-down. … JTX_FORCE_LANE_PD[1] = Lane 1 force power-down. JTX_FORCE_LANE_PD[0] = Lane 0 force power-down.	0x0	R/W
0x53C	JTX_LANE_PDWN2	[7:0]	JTX_FORCE_LANE_PD[15:8]		Physical Lane Force Power Down. 16-bit bit fields are split into two registers. JTX_FORCE_LANE_PD[15] = Lane 15 force power-down. JTX_FORCE_LANE_PD[14] = Lane 14 force power-down. … JTX_FORCE_LANE_PD[9] = Lane 9 force power-down. JTX_FORCE_LANE_PD[8] = Lane 8 force power-down.	0x0	R/W
0x53D	JTX_LANE_ASSIGN1	[7:4]	JTX_LANE_ASSIGN_1		Physical Lane 1 Assignment.	0x1	R/W
				0000	Logical Lane 0.		
				0001	Logical Lane 1 (default).		
				0010	Logical Lane 2.		
				0011	Logical Lane 3.		
				0100	Logical Lane 4.		
				0101	Logical Lane 5.		
				0110	Logical Lane 6.		
				0111	Logical Lane 7.		
				1000	Logical Lane 8.		
				1001	Logical Lane 9.		

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
				1010	Logical Lane 10.		
				1011	Logical Lane 11.		
				1100	Logical Lane 12.		
				1101	Logical Lane 13.		
				1110	Logical Lane 14.		
				1111	Logical Lane 15.		
		[3:0]	JTX_LANE_ASSIGN_0		Physical Lane 0 Assignment.	0x0	R/W
				0000	Logical Lane 0 (default).		
				0001	Logical Lane 1.		
				0010	Logical Lane 2.		
				0011	Logical Lane 3.		
				0100	Logical Lane 4.		
				0101	Logical Lane 5.		
				0110	Logical Lane 6.		
				0111	Logical Lane 7.		
				1000	Logical Lane 8.		
				1001	Logical Lane 9.		
				1010	Logical Lane 10.		
				1011	Logical Lane 11.		
				1100	Logical Lane 12.		
				1101	Logical Lane 13.		
				1110	Logical Lane 14.		
				1111	Logical Lane 15.		
0x53E	JTX_LANE_ASSIGN2	[7:4]	JTX_LANE_ASSIGN_3		Physical Lane 3 Assignment.	0x3	R/W
				0000	Logical Lane 0.		
				0001	Logical Lane 1.		
				0010	Logical Lane 2.		
				0011	Logical Lane 3 (default).		
				0100	Logical Lane 4.		
				0101	Logical Lane 5.		
				0110	Logical Lane 6.		
				0111	Logical Lane 7.		
				1000	Logical Lane 8.		
				1001	Logical Lane 9.		
				1010	Logical Lane 10.		
				1011	Logical Lane 11.		
				1100	Logical Lane 12.		
				1101	Logical Lane 13.		
				1110	Logical Lane 14.		
				1111	Logical Lane 15.		
		[3:0]	JTX_LANE_ASSIGN_2		Physical Lane 2 Assignment.	0x2	R/W
				0000	Logical Lane 0.		
				0001	Logical Lane 1.		
				0010	Logical Lane 2 (default).		
				0011	Logical Lane 3.		
				0100	Logical Lane 4.		
				0101	Logical Lane 5.		
				0110	Logical Lane 6.		
				0111	Logical Lane 7.		
				1000	Logical Lane 8.		
				1001	Logical Lane 9.		
				1010	Logical Lane 10.		
				1011	Logical Lane 11.		
				1100	Logical Lane 12.		
				1101	Logical Lane 13.		
				1110	Logical Lane 14.		
				1111	Logical Lane 15.		

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x53F	JTX_LANE_ASSIGN3	[7:4]	JTX_LANE_ASSIGN_5		Physical Lane 5 Assignment.	0x5	R/W
				0000	Logical Lane 0.		
				0001	Logical Lane 1.		
				0010	Logical Lane 2.		
				0011	Logical Lane 3.		
				0100	Logical Lane 4.		
				0101	Logical Lane 5 (default).		
				0110	Logical Lane 6.		
				0111	Logical Lane 7.		
				1000	Logical Lane 8.		
				1001	Logical Lane 9.		
				1010	Logical Lane 10.		
				1011	Logical Lane 11.		
				1100	Logical lane 12.		
				1101	Logical lane 13.		
				1110	Logical lane 14.		
				1111	Logical lane 15.		
		[3:0]	JTX_LANE_ASSIGN_4		Physical Lane 4 Assignment.	0x4	R/W
				0000	Logical Lane 0.		
				0001	Logical Lane 1.		
				0010	Logical Lane 2.		
				0011	Logical Lane 3.		
				0100	Logical Lane 4 (default).		
				0101	Logical Lane 5.		
				0110	Logical Lane 6.		
				0111	Logical Lane 7.		
				1000	Logical Lane 8.		
				1001	Logical Lane 9.		
				1010	Logical Lane 10.		
				1011	Logical Lane 11.		
				1100	Logical Lane 12.		
				1101	Logical Lane 13.		
				1110	Logical Lane 14.		
				1111	Logical Lane 15.		
0x540	JTX_LANE_ASSIGN4	[7:4]	JTX_LANE_ASSIGN_7		Physical Lane 7 Assignment.	0x7	R/W
				0000	Logical Lane 0.		
				0001	Logical Lane 1.		
				0010	Logical Lane 2.		
				0011	Logical Lane 3.		
				0100	Logical Lane 4.		
				0101	Logical Lane 5.		
				0110	Logical Lane 6.		
				0111	Logical Lane 7 (default).		
				1000	Logical Lane 8.		
				1001	Logical Lane 9.		
				1010	Logical Lane 10.		
				1011	Logical Lane 11.		
				1100	Logical Lane 12.		
				1101	Logical Lane 13.		
				1110	Logical Lane 14.		
				1111	Logical Lane 15.		
		[3:0]	JTX_LANE_ASSIGN_6		Physical Lane 6 Assignment.	0x6	R/W
				0000	Logical Lane 0.		
				0001	Logical Lane 1.		
				0010	Logical Lane 2.		
				0011	Logical Lane 3.		
				0100	Logical Lane 4.		
				0101	Logical Lane 5.		
				0110	Logical Lane 6 (default).		

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
				0111	Logical Lane 7.		
				1000	Logical Lane 8.		
				1001	Logical Lane 9.		
				1010	Logical Lane 10.		
				1011	Logical Lane 11.		
				1100	Logical Lane 12.		
				1101	Logical Lane 13.		
				1110	Logical Lane 14.		
				1111	Logical Lane 15.		
0x541	JTX_LANE_ASSIGN5	[7:4]	JTX_LANE_ASSIGN_9		Physical Lane 9 Assignment.	0x9	R/W
				0000	Logical Lane 0.		
				0001	Logical Lane 1.		
				0010	Logical Lane 2.		
				0011	Logical Lane 3.		
				0100	Logical Lane 4.		
				0101	Logical Lane 5.		
				0110	Logical Lane 6.		
				0111	Logical Lane 7.		
				1000	Logical Lane 8.		
				1001	Logical Lane 9 (default).		
				1010	Logical Lane 10.		
				1011	Logical Lane 11.		
				1100	Logical Lane 12.		
				1101	Logical Lane 13.		
				1110	Logical Lane 14.		
				1111	Logical Lane 15.		
		[3:0]	JTX_LANE_ASSIGN_8		Physical Lane 8 Assignment.	0x8	R/W
				0000	Logical Lane 0.		
				0001	Logical Lane 1.		
				0010	Logical Lane 2.		
				0011	Logical Lane 3.		
				0100	Logical Lane 4.		
				0101	Logical Lane 5.		
				0110	Logical Lane 6.		
				0111	Logical Lane 7.		
				1000	Logical Lane 8 (default).		
				1001	Logical Lane 9.		
				1010	Logical Lane 10.		
				1011	Logical Lane 11.		
				1100	Logical Lane 12.		
				1101	Logical Lane 13.		
				1110	Logical Lane 14.		
				1111	Logical Lane 15.		
0x542	JTX_LANE_ASSIGN6	[7:4]	JTX_LANE_ASSIGN_11		Physical Lane 11 Assignment.	0xB	R/W
				0000	Logical Lane 0.		
				0001	Logical Lane 1.		
				0010	Logical Lane 2.		
				0011	Logical Lane 3.		
				0100	Logical Lane 4.		
				0101	Logical Lane 5.		
				0110	Logical Lane 6.		
				0111	Logical Lane 7.		
				1000	Logical Lane 8.		
				1001	Logical Lane 9.		
				1010	Logical Lane 10.		
				1011	Logical Lane 11 (default).		
				1100	Logical Lane 12.		

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
				1101	Logical Lane 13.		
				1110	Logical Lane 14.		
				1111	Logical Lane 15.		
		[3:0]	JTX_LANE_ASSIGN_10		Physical Lane 10 Assignment.	0xA	R/W
				0000	Logical Lane 0.		
				0001	Logical Lane 1.		
				0010	Logical Lane 2.		
				0011	Logical Lane 3.		
				0100	Logical Lane 4.		
				0101	Logical Lane 5.		
				0110	Logical Lane 6.		
				0111	Logical Lane 7.		
				1000	Logical Lane 8.		
				1001	Logical Lane 9.		
				1010	Logical Lane 10 (default).		
				1011	Logical Lane 11.		
				1100	Logical Lane 12.		
				1101	Logical Lane 13.		
				1110	Logical Lane 14.		
				1111	Logical Lane 15.		
0x543	JTX_LANE_ASSIGN7	[7:4]	JTX_LANE_ASSIGN_13		Physical Lane 13 Assignment.	0xD	R/W
				0000	Logical Lane 0.		
				0001	Logical Lane 1.		
				0010	Logical Lane 2.		
				0011	Logical Lane 3.		
				0100	Logical Lane 4.		
				0101	Logical Lane 5.		
				0110	Logical Lane 6.		
				0111	Logical Lane7.		
				1000	Logical Lane 8.		
				1001	Logical Lane 9.		
				1010	Logical Lane 10.		
				1011	Logical Lane 11.		
				1100	Logical Lane 12.		
				1101	Logical Lane 13 (default).		
				1110	Logical Lane 14.		
				1111	Logical Lane 15.		
		[3:0]	JTX_LANE_ASSIGN_12		Physical Lane 12 Assignment.	0xC	R/W
				0000	Logical Lane 0.		
				0001	Logical Lane 1.		
				0010	Logical Lane 2.		
				0011	Logical Lane 3.		
				0100	Logical Lane 4.		
				0101	Logical Lane 5.		
				0110	Logical Lane 6.		
				0111	Logical Lane 7.		
				1000	Logical Lane 8.		
				1001	Logical Lane 9.		
				1010	Logical Lane 10.		
				1011	Logical Lane 11.		
				1100	Logical Lane 12 (default).		
				1101	Logical Lane 13.		
				1110	Logical Lane 14.		
				1111	Logical Lane 15.		
0x544	JTX_LANE_ASSIGN8	[7:4]	JTX_LANE_ASSIGN_15		Physical Lane 15 Assignment.	0xF	R/W
				0000	Logical Lane 0.		
				0001	Logical Lane 1.		
				0010	Logical Lane 2.		
				0011	Logical Lane 3.		

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
				0100	Logical Lane 4.		
				0101	Logical Lane 5.		
				0110	Logical Lane 6.		
				0111	Logical Lane 7.		
				1000	Logical Lane 8.		
				1001	Logical Lane 9.		
				1010	Logical Lane 10.		
				1011	Logical Lane 11.		
				1100	Logical Lane 12.		
				1101	Logical Lane 13.		
				1110	Logical Lane 14.		
				1111	Logical Lane 15 (default).		
		[3:0]	JTX_LANE_ASSIGN_14		Physical Lane 14 Assignment.	0xE	R/W
				0000	Logical Lane 0.		
				0001	Logical Lane 1.		
				0010	Logical Lane 2.		
				0011	Logical Lane 3.		
				0100	Logical Lane 4.		
				0101	Logical Lane 5.		
				0110	Logical Lane 6.		
				0111	Logical Lane 7.		
				1000	Logical Lane 8.		
				1001	Logical Lane 9.		
				1010	Logical Lane 10.		
				1011	Logical Lane 11.		
				1100	Logical Lane 12.		
				1101	Logical Lane 13.		
				1110	Logical Lane 14 (default).		
				1111	Logical Lane 15.		
0x547	JTX_QBF_STATUS	[7:0]	JTX_QBF_STATUS		QBF Status	0x7D	R
0x557	JTX_TEST_GEN_INV	[7:1]	Reserved		Reserved.	0x0	R
		0	JTX_TEST_GEN_INV		JESD Test Generator Invert.	0x0	R/W
				0	Normal test mode data.		
				1	Inverted test mode data.		
0x558	CHIP_USR_PAT_1_7_0	[7:0]	CHIP_USR_PAT_1_7_0		CHIP_USR_PAT_1. 8 LSBs of User Pattern 1.	0x0	R/W
0x559	CHIP_USR_PAT_1_15_8	[7:0]	CHIP_USR_PAT_1_15_8		CHIP_USR_PAT_1. 8 MSBs of User Pattern 1.	0x0	R/W
0x55A	CHIP_USR_PAT_2_7_0	[7:0]	CHIP_USR_PAT_2_7_0		CHIP_USR_PAT_2. 8 LSBs of User Pattern 2.	0x0	R/W
0x55B	CHIP_USR_PAT_2_15_8	[7:0]	CHIP_USR_PAT_2_15_8		CHIP_USR_PAT_2. 8 MSBs of User Pattern 2.	0x0	R/W
0x55C	CHIP_USR_PAT_3_7_0	[7:0]	CHIP_USR_PAT_3_7_0		CHIP_USR_PAT_3. 8 LSBs of User Pattern 3.	0x0	R/W
0x55D	CHIP_USR_PAT_3_15_8	[7:0]	CHIP_USR_PAT_3_15_8		CHIP_USR_PAT_3. 8 MSBs of User Pattern 3.	0x0	R/W
0x55E	CHIP_USR_PAT_4_7_0	[7:0]	CHIP_USR_PAT_4_7_0		CHIP_USR_PAT_4. 8 LSBs of User Pattern 4.	0x0	R/W
0x55F	CHIP_USR_PAT_4_15_8	[7:0]	CHIP_USR_PAT_4_15_8		CHIP_USR_PAT_4. 8 MSBs of User Pattern 4.	0x0	R/W
0x560	SER_PARITY_RESET_EN1	[7:0]	SER_PARITY_RESET_EN[7:0]		Parity Reset Enable, Bits[7:0].	0x0	R/W
0x561	SER_PARITY_RESET_EN2	[7:0]	SER_PARITY_RESET_EN[15:8]		Parity Reset Enable, Bits[15:8].	0x0	R/W
0x564	SER_PARITY_ERR1	[7:0]	SER_PARITY_ERR[7:0]		Parity Error, Bits[7:0].	0x0	R
0x565	SER_PARITY_ERR2	[7:0]	SER_PARITY_ERR[15:8]		Parity Error, Bits[15:8].	0x0	R
0x570	PLL_ENABLE_CTRL	[7:5]	Reserved		Reserved.	0x0	R
		4	LOLSTICKYCLEAR_FORCE_LCPLL_RC		Clears Out Loss of Lock Bit	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		2	LDSYNTH_FORCE_LCPLL_ADC		A short 1 pulse starts VCO calibration, the pulse width must be at least one reference clock period. Allows user to perform a calibration at will.	0x0	R/W
		1	RESERVED		Reserved.	0x0	R
		0	PWRUP_LCPLL		Power Up SERDES PLL.	0x1	R/W
				0	SERDES PLL powered off.		
				1	SERDES PLL powered on.		

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x5B0	PWR_DN	[7:0]	PD_SER[7:0]		PHY Channel Power Down. Active high, <0> = Channel 0, <1> = Channel 1 …	0x00	R/W
0x5B1	PWR_DN2	[7:0]	PD_SER[15:8]		PHY Channel Power Down. Active high, <0> = Channel 0, <1> = Channel 1 …	0x00	R/W
0x5B2	JTX_SWING1	7	Reserved		Reserved.	0x0	R
		[6:4]	DRVSWING_CH1_SER_RC		Output Voltage Swing Level for JESD204B.	0x1	R/W
				0	1.0 × V_{JVTT}.		
				1	0.850 × V_{JVTT}.		
				2	0.750 × V_{JVTT}.		
				3	0.500 × V_{JVTT}.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	DRVSWING_CH0_SER_RC		Output Voltage Swing Level for JESD204B.	0x1	R/W
				0	1.0 × V_{JVTT}.		
				1	0.850 × V_{JVTT}.		
				2	0.750 × V_{JVTT}.		
				3	0.500 × V_{JVTT}.		
0x5B3	JTX_SWING2	7	Reserved		Reserved.	0x0	R
		[6:4]	DRVSWING_CH3_SER_RC		Output Voltage Swing Level for JESD204B.	0x1	R/W
				0	1.0 × V_{JVTT}.		
				1	0.850 × V_{JVTT}.		
				2	0.750 × V_{JVTT}.		
				3	0.500 × V_{JVTT}.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	DRVSWING_CH2_SER_RC		Output Voltage Swing Level for JESD204B.	0x1	R/W
				0	1.0 × V_{JVTT}.		
				1	0.850 × V_{JVTT}.		
				2	0.750 × V_{JVTT}.		
				3	0.500 × V_{JVTT}.		
0x5B4	JTX_SWING3	7	Reserved		Reserved.	0x0	R
		[6:4]	DRVSWING_CH5_SER_RC		Output Voltage Swing Level for JESD204B.	0x1	R/W
				0	1.0 × V_{JVTT}.		
				1	0.850 × V_{JVTT}.		
				2	0.750 × V_{JVTT}.		
				3	0.500 × V_{JVTT}.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	DRVSWING_CH4_SER_RC		Output Voltage Swing Level for JESD204B.	0x1	R/W
				0	1.0 × V_{JVTT}.		
				1	0.850 × V_{JVTT}.		
				2	0.750 × V_{JVTT}.		
				3	0.500 × V_{JVTT}.		
0x5B5	JTX_SWING4	7	Reserved		Reserved.	0x0	R
		[6:4]	DRVSWING_CH7_SER_RC		Output Voltage Swing Level for JESD204B.	0x1	R/W
				0	1.0 × V_{JVTT}.		
				1	0.850 × V_{JVTT}.		
				2	0.750 × V_{JVTT}.		
				3	0.500 × V_{JVTT}.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	DRVSWING_CH6_SER_RC		Output Voltage Swing Level for JESD204B.	0x1	R/W
				0	1.0 × V_{JVTT}.		
				1	0.850 × V_{JVTT}.		
				2	0.750 × V_{JVTT}.		
				3	0.500 × V_{JVTT}.		
0x5B6	JTX_SWING5	7	Reserved		Reserved.	0x0	R
		[6:4]	DRVSWING_CH9_SER_RC		Output Voltage Swing Level for JESD204B.	0x1	R/W
				0	1.0 × V_{JVTT}.		
				1	0.850 × V_{JVTT}.		
				2	0.750 × V_{JVTT}.		
				3	0.500 × V_{JVTT}.		

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
		3	Reserved		Reserved.	0x0	R
		[2:0]	DRVSWING_CH8_SER_RC		Output Voltage Swing Level for JESD204B.	0x1	R/W
				0	1.0 × V_{JVTT}.		
				1	0.850 × V_{JVTT}.		
				2	0.750 × V_{JVTT}.		
				3	0.500 × V_{JVTT}.		
0x5B7	JTX_SWING6	7	Reserved		Reserved.	0x0	R
		[6:4]	DRVSWING_CH11_SER_RC		Output Voltage Swing Level for JESD204B.	0x1	R/W
				0	1.0 × V_{JVTT}.		
				1	0.850 × V_{JVTT}.		
				2	0.750 × V_{JVTT}.		
				3	0.500 × V_{JVTT}.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	DRVSWING_CH10_SER_RC		Output Voltage Swing Level for JESD204B.	0x1	R/W
				0	1.0 × V_{JVTT}.		
				1	0.850 × V_{JVTT}.		
				2	0.750 × V_{JVTT}.		
				3	0.500 × V_{JVTT}.		
0x5B8	JTX_SWING7	7	Reserved		Reserved.	0x0	R
		[6:4]	DRVSWING_CH13_SER_RC		Output Voltage Swing Level for JESD204B.	0x1	R/W
				0	1.0 × V_{JVTT}.		
				1	0.850 × V_{JVTT}.		
				2	0.750 × V_{JVTT}.		
				3	0.500 × V_{JVTT}.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	DRVSWING_CH12_SER_RC		Output Voltage Swing Level for JESD204B.	0x1	R/W
				0	1.0 × V_{JVTT}.		
				1	0.850 × V_{JVTT}.		
				2	0.750 × V_{JVTT}.		
				3	0.500 × V_{JVTT}.		
0x5B9	JTX_SWING8	7	Reserved		Reserved.	0x0	R
		[6:4]	DRVSWING_CH15_SER_RC		Output Voltage Swing Level for JESD204B.	0x1	R/W
				0	1.0 × V_{JVTT}.		
				1	0.850 × V_{JVTT}.		
				2	0.750 × V_{JVTT}.		
				3	0.500 × V_{JVTT}.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	DRVSWING_CH14_SER_RC		Output Voltage Swing Level for JESD204B.	0x1	R/W
				0	1.0 × V_{JVTT}.		
				1	0.850 × V_{JVTT}.		
				2	0.750 × V_{JVTT}.		
				3	0.500 × V_{JVTT}.		
0x5BA	SERDOUT0/SERDOUT1 de-emphasis select	7	Reserved		Reserved.	0x0	R
		[6:4]	SERDOUT1		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
				3	9 dB.		
				4	12 dB.		
				5 to 7	Not applicable.		
		3	Reserved		Reserved.	0x0	R

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
		[2:0]	SERDOUT0		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
				3	9 dB.		
				4	12 dB.		
				5 to 7	Not applicable.		
0x5BB	SERDOUT2/SERDOUT3 de-emphasis select	7	Reserved		Reserved.	0x0	R
		[6:4]	SERDOUT3		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
				3	9 dB.		
				4	12 dB.		
				5 to 7	Not applicable.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT2		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
				3	9 dB.		
				4	12 dB.		
				5 to 7	Not applicable.		
0x5BC	SERDOUT4/SERDOUT5 de-emphasis select	7	Reserved		Reserved.	0x0	R
		[6:4]	SERDOUT5		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
				3	9 dB.		
				4	12 dB.		
				5 to 7	Not applicable.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT4		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
				3	9 dB.		
				4	12 dB.		
				5 to 7	Not applicable.		
0x5BD	SERDOUT6/SERDOUT7 de-emphasis select	7	Reserved		Reserved.	0x0	R
		[6:4]	SERDOUT7		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
				3	9 dB.		
				4	12 dB.		
				5 to 7	Not applicable.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT6		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
				3	9 dB.		
				4	12 dB.		
				5 to 7	Not applicable.		

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x5BE	SERDOUT8/SERDOUT9 de-emphasis select	7	Reserved		Reserved.	0x0	R
		[6:4]	SERDOUT9		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
				3	9 dB.		
				4	12 dB.		
				5 to 7	Not applicable.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT8		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
				3	9 dB.		
				4	12 dB.		
				5 to 7	Not applicable.		
0x5BF	SERDOUT10/SERDOUT11 de-emphasis select	7	Reserved		Reserved.	0x0	R
		[6:4]	SERDOUT11		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
				3	9 dB.		
				4	12 dB.		
				5 to 7	Not applicable.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT10		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
				3	9 dB.		
				4	12 dB.		
				5 to 7	Not applicable.		
0x5C0	SERDOUT12/SERDOUT13 de-emphasis select	7	Reserved		Reserved.	0x0	R
		[6:4]	SERDOUT13		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
				3	9 dB.		
				4	12 dB.		
				5 to 7	Not applicable.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT12		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
				3	9 dB.		
				4	12 dB.		
				5 to 7	Not applicable.		
0x5C1	SERDOUT14/SERDOUT15 de-emphasis select	7	Reserved		Reserved.	0x0	R
		[6:4]	SERDOUT15		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
				3	9 dB.		
				4	12 dB.		
				5 to 7	Not applicable.		
		3	Reserved		Reserved.	0x0	R

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
		[2:0]	SERDOUT14		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
				3	9 dB.		
				4	12 dB.		
				5 to 7	Not applicable.		
0x5EA	MAIN_DATA_INV	7	OUTPUTDATAINVERT_CH7_SER_RC		JTx, Invert Channel 7 Data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		6	OUTPUTDATAINVERT_CH6_SER_RC		JTx, Invert Channel 6 Data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		5	OUTPUTDATAINVERT_CH5_SER_RC		JTx, Invert Channel 5 Data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		4	OUTPUTDATAINVERT_CH4_SER_RC		JTx, Invert Channel 4 Data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		3	OUTPUTDATAINVERT_CH3_SER_RC		JTx, Invert Channel 3 Data.	0x0	R/W
				0	Normal.		
				1	INVERT.		
		2	OUTPUTDATAINVERT_CH2_SER_RC		JTx, Invert Channel 2 Data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		1	OUTPUTDATAINVERT_CH1_SER_RC		JTx, Invert Channel 1 Data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		0	OUTPUTDATAINVERT_CH0_SER_RC		JTx, Invert Channel 0 Data.	0x0	R/W
				0	Normal.		
				1	Invert.		
0x5EB	MAIN_DATA_INV2	7	OUTPUTDATAINVERT_CH15_SER_RC		JTx, Invert Channel 15 Data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		6	OUTPUTDATAINVERT_CH14_SER_RC		JTx, Invert Channel 14 Data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		5	OUTPUTDATAINVERT_CH13_SER_RC		JTx, Invert Channel 13 Data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		4	OUTPUTDATAINVERT_CH12_SER_RC		JTx, Invert Channel 12 Data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		3	OUTPUTDATAINVERT_CH11_SER_RC		JTx, Invert Channel 11 Data	0x0	R/W
				0	Normal.		
				1	Invert.		

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
		2	OUTPUTDATAINVERT_ CH10_SER_RC		JTx, Invert Channel 10 Data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		1	OUTPUTDATAINVERT_ CH9_SER_RC		JTx, Invert Channel 9 Data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		0	OUTPUTDATAINVERT_ CH8_SER_RC		JTx, Invert Channel 8 Data.	0x0	R/W
				0	Normal.		
				1	Invert.		
0x600	DDC_SYNC_CTRL	7	DDC_TRIG_NCO_ RESET_EN		DDC Trigger NCO Reset Enable.	0x0	R/W
		[6:5]	Reserved		Reserved.	0x0	R
		4	DDC_SOFT_RESET		Digital Down Converter Soft Reset. Note: this bit can be used to synchronize all NCOs inside the DDC blocks.	0x0	R/W
				0	Normal operation.		
				1	DDC held in reset.		
		[3:2]	Reserved		Reserved.	0x0	R
		1	DDC_SYNC_NEXT		DDC Next Synchronization Mode. Used only when DDC_SYNC_EN = 1 or DDC_TRIG_ NCO_RESET_EN =1. Both must not be set to 1 at any given time.	0x1	R/W
				0	Continuous mode. The SYSREF frequency must be an integer multiple of the NCO frequency for this function to operate correctly in continuous mode.		
				1	Synchronization mode. Only the next valid edge of SYSREF_x pin are used to synchronize the NCO in the DDC block. Subsequent edges of the SYSREF_x pin are ignored until DDC_SYNC_EN bit has been cleared and set again.		
		0	DDC_SYNC_EN		DDC Synchronization Enable.	0x0	R/W
				0	Synchronization disabled.		
				1	Synchronization enabled. If DDC_SYNC_ NEXT = 1, only the next valid edge of the SYSREF_x pin is used to synchronize the NCO in the DDC block. Subsequent edges of the SYSREF_x pin are ignored. When the next SYSREF_x edge is received, DDC_SYNC_EN bit must be cleared for any subsequent use of the next SYSREF_x edge.		
0x601	DDC_SYNC_STATUS	[7:1]	Reserved		Reserved.	0x0	R
		0	DDC_SYNC_EN_CLEAR		DDC Synchronization Enable Clear Status	0x0	R
0x602	DDC_TRIG_CTRL	[7:1]	Reserved		Reserved.	0x0	R
		0	DDC_TRIG_HOP_EN		DDC TRIG_x Hop Enable.	0x0	R/W
				0	Frequency hopping is independent of TRIG_x signal.		
				1	TRIG_x signal used for frequency hopping. When disabled, frequency hopping is based on a channel selection decoded from the register map or GPIO. For a single channel, PHASE_INC and PHASE_OFFSET are written into an active channel shadow register.		
0x606	CHIP_DP_MODE	[7:6]	Reserved		Reserved.	0x0	R
		5	CHIP_I_ONLY		Real (I) Selection.	0x0	R/W
				0	Real (I) and complex (Q) selected.		
				1	Only Real (I) selected. Complex (Q) is ignored.		
		4	Reserved		Reserved.	0x0	R

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
		[3:0]	CHIP_DP_APP_MODE		Chip Application Layer Operation Mode.	0x0	R/W
				0x0	Full bandwidth mode (high performance mode).		
				0x1	One DDC mode (DDC 0 only).		
				0x2 to 0xF	Unused.		
0x607	CHIP_DEC_RATIO	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	CHIP_DEC_RATIO		Chip Decimation Ratio.	0x0	R/W
				0x0	Full sample rate (decimate by 1).		
				0x1	Decimate by 2 ratio.		
				0x2	Decimate by 4 ratio.		
				0x3	Decimate by 8 ratio.		
				0x4	Decimate by 16 ratio.		
				0x5	Decimate by 32 ratio.		
				0x6	Decimate by 64 ratio.		
				0x7	Decimate by 128 ratio.		
				0x8	Reserved.		
				0x9	Decimate by 3 ratio.		
				0xA	Decimate by 6 ratio.		
				0xB	Decimate by 12 ratio.		
				0xC	Decimate by 24 ratio.		
				0xD	Decimate by 48 ratio.		
				0xE	Decimate by 96 ratio.		
				0xF	Reserved.		
0x608	CHIP_RES_0	[7:4]	CHIP_CONV_RES_0		Chip Converter Resolution 0, Bits[7:4]. Chip converter resolution for Application Layer Mode 0 (high performance mode).	0x0	R/W
				0x0	16-bit resolution.		
				0x1	15-bit resolution.		
					…		
				0x9	7-bit resolution.		
				0xA to 0xF	Reserved.		
		[3:0]	CHIP_OUT_RES_0		Chip Out Resolution 0, Bits[3:0]. Chip output resolution for Application Layer Mode 0 (high performance mode).	0x0	R/W
				0x0	16-bit resolution.		
				0x1	15-bit resolution.		
					…		
				0x9	7-bit resolution		
				0xA to 0xF	Reserved.		
0x609	CHIP_RES_1	[7:4]	CHIP_CONV_RES_1		Chip Converter Resolution 1, Bits[7:4]. Chip converter resolution for Application Layer Mode 1	0x0	R/W
				0x0	16-bit resolution.		
				0x1	15-bit resolution.		
					…		
				0x9	7-bit resolution		
				0xA to 0xF	Reserved.		
		[3:0]	CHIP_OUT_RES_1		Chip Out Resolution 1, Bits[3:0]. Chip output resolution for Application Layer Mode 1.	0x0	R/W
				0x0	16-bit resolution.		
				0x1	15-bit resolution.		
					…		
				0x9	7-bit resolution		
				0xA to 0xF	Reserved.		
0x620	CTRL_0_1_SEL	[7:4]	DFORMAT_CTRL_BIT_1_SEL		Control Bit 1 Mux Selection.	0x0	R/W
				0x0	Overrange bit.		
				0x1	Tie low (1'b0).		
				0x2	Signal monitor (SMON) bit.		
				0x3	Fast detect (FD) bit.		

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
				0x4	Reserved.		
				0x5	SYSREF_x.		
				0x6	Reserved.		
				0x7	Reserved.		
				0x8	NCO channel selection, Bit 0.		
				0x9	NCO channel selection, Bit 1.		
				0xA	NCO channel selection, Bit 2.		
				0xB	NCO channel selection, Bit 3.		
		[3:0]	DFORMAT_CTRL_BIT_0_SEL		Control Bit 0 Mux Selection.	0x0	R/W
				0x0	Overrange bit.		
				0x1	Tie low (1'b0).		
				0x2	SMON bit.		
				0x3	FD bit.		
				0x4	Reserved.		
				0x5	SYSREF_x.		
				0x6	Reserved.		
				0x7	Reserved.		
				0x8	NCO channel selection, Bit 0.		
				0x9	NCO channel selection, Bit 1.		
				0xA	NCO channel selection, Bit 2.		
				0xB	NCO channel selection, Bit 3.		
0x621	CTRL_2_SEL	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DFORMAT_CTRL_BIT_2_SEL		Control Bit 2 Mux Selection.	0x0	R/W
				0x0	Overrange bit.		
				0x1	Tie low (1'b0).		
				0x2	SMON bit.		
				0x3	FD bit.		
				0x4	Reserved.		
				0x5	SYSREF_x.		
				0x6	Reserved.		
				0x7	Reserved.		
				0x8	NCO channel selection, Bit 0.		
				0x9	NCO channel selection, Bit 1.		
				0xA	NCO channel selection, Bit 2.		
				0xB	NCO channel selection, Bit 3.		
0x622	OUT_FORMAT_SEL	[7:3]	Reserved		Reserved.	0x0	R
		2	DFORMAT_INV		Output Data Inversion Enable. Digital ADC sample invert.	0x0	R/W
				0	ADC sample data is NOT inverted		
				1	ADC sample data is inverted		
		[1:0]	DFORMAT_SEL		Output Data Format Selection. Digital ADC data format select (DFS)	0x0	R/W
				00	Twos complement (default).		
				01	Offset binary.		
				10	Gray code.		
				11	Reserved.		
0x623	OVR_STATUS	[7:2]	Reserved		Reserved.	0x0	R
		[1:0]	DFORMAT_OVR_STATUS		Output Overrange Status Indicator. Converter overrange indication sticky bits (active high). One bit for each virtual converter. This bit is set to 1 if converter is driven beyond the specified input range and is sticky (remains set) until explicitly cleared by writing 1 to the corresponding DFORMAT_OVR_CLEAR[1:0] bit. The corresponding DFORMAT_OVR_CLEAR[1:0] bit must be cleared for further overflows to be reported Bit 0: overrange sticky bit for Converter 0. Bit 1: overrange sticky bit for Converter 1.	0x0	R

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
				0	No overrange.		
				1	Overrange occurred.		
0x624	OVR_CLR	[7:2]	Reserved		Reserved.	0x0	R
		[1:0]	DFORMAT_OVR_CLR		Overrange Status Clear. Converter overrange clear bit (active high). When an overrange sticky bit has been set, it remains set until explicitly cleared by writing 1 to the corresponding DFORMAT_OVR_CLEAR[1:0] bit. The DFORMAT_OVR_CLEAR[1:0] bit must be cleared for further overrange to be reported. Bit 0: overrange sticky bit clear for Converter 0. Bit 1: overrange sticky bit clear for Converter 1.	0x0	R/W
0x625	OUT_CHAN_SEL	[7:2]	Reserved		Reserved.	0x0	R
		1	DFORMAT_CHAN_REPLICATE		Output Channel Replication Control.	0x0	R/W
				0	Unused converter outputs are zero.		
				1	Unused converter outputs are replicas of valid converter outputs. For example, when in high performance mode (CHIP_APP_MODE = 0x0), Converter 1 is unused. When this bit is set, Converter 0 is replicated on Converter 1.		
		0	DFORMAT_CHAN_SWAP		Output Converter Channel Swap Control.	0x0	R/W
				0	Normal channel ordering.		
				1	Channel Swap Enabled. Converter 0 and Converter 1 are swapped.		
0x626	OUT_RES	[7:5]	Reserved		Reserved.	0x0	R
		4	DFORMAT_FBW_DITHER_EN		DFORMAT Full Bandwidth (FBW) Dither Enable. DFORMAT dither enable/disable for mode.	0x0	R/W
				0	Dither disable.		
				1	Dither enable.		
		[3:0]	DFORMAT_RES		Data Output Resolution.	0x0	R/W
				0x0	16-bit resolution.		
				0x1	15-bit resolution.		
					…		
				0x9	7-bit resolution.		
				0xA to 0xF	Reserved.		
0x630	DDC_CTRL	[7:5]	Reserved		Reserved.	0x0	R
		4	DDC0_C2R_EN		Complex to Real Enable.	0x0	R/W
				0	Complex (I and Q) outputs contain valid data.		
				1	Real (I) output only. Complex to real enabled. Uses extra $f_S/4$ mixing to convert to real.		
		[3:2]	DDC0_IF_MODE		DDC Intermediate Frequency (IF) Mode.	0x0	R/W
				00	Variable IF mode. Mixers and NCO enabled. Use DDC_PHASE_INC[11:0] to digitally tune the IF frequency.		
				01	0 Hz IF mode. Mixers bypassed and NCO disabled. This mode infers clock gating cells inside the Mixer and the NCO, and gates combinatorial logic in the mixer multiplier to save dynamic logic.		
				10	$f_S/4$ Hz IF mode. Mixers and NCO are enabled in special down-mixing by $f_S/4$ mode. This power saving mode is described in more detail in the JESD204B standard, Section 1.1.6.1.6. $f_S/4$ IF mode gain is different in this mode than in variable IF mode $f_S/4$.		

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
				11	Test mode. Input samples are forced to +0.999… (positive full scale). The NCO is enabled, and this test mode allows the NCOs to directly drive the decimation filters and is useful when evaluating the performance of the NCOs and decimation filters.		
		1	DDC0_GAIN		Gain Selection. Note that gain can be used to compensate for the 6 dB loss associated with mixing an input signal down to baseband and filtering out its negative component.	0x0	R/W
				0	0 dB gain.		
				1	6 dB gain (multiply by 2).		
		0	Reserved		Reserved.	0x0	R
0x631	DDC_DEC_CTRL	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DDC0_DEC_SEL		Decimation Ratio Selection.	0x0	R/W
				0	Decimate by 2.		
				1	Decimate by 4.		
				2	Decimate by 8.		
				3	Decimate by 16.		
				4	Decimate by 32.		
				5	Decimate by 64.		
				6	Decimate by 128.		
				7	Reserved.		
				8	Decimate by 6.		
				9	Decimate by 12.		
				10	Decimate by 24.		
				11	Decimate by 48.		
				12	Decimate by 96.		
				13	Reserved.		
				14	Reserved.		
				15	Reserved.		
0x632	DDC_NCO_CTRL	[7:4]	DDC0_NCO_CHAN_SEL_MODE		NCO Channel Selection Mode. Note that for edge control/frequency hop timer (FHT)-based control, the internal counter wraps when the DDC_NCO_REGMAP_CHAN_SEL value is reached.	0x0	R/W
				0000	Register map control (use DDC_NCO_REGMAP_CHAN_SEL).		
				0001	PROFILE_PINS[0] used. Pin level control (3'b0, PROFILE_PINS[0]).		
				0010	PROFILE_PINS[1:0] used. Pin level control (2'b0, PROFILE_PINS[1:0]).		
				0011	PROFILE_PINS[2:0] are used. Pin level control (1'b0, PROFILE_PINS[2:0]).		
				0100	PROFILE_PINS[3:0] are used. Pin level control (PROFILE_PINS[3:0]).		
				0101 to 0111	Reserved		
				1000	PROFILE_PINS[0]. Pin edge control, increments internal counter when rising edge of PROFILE_PINS[0].		
				1100	FHT expire based control. Increment internal counter when FHT is expired.		
				1101 to 1111	Reserved		
		[3:0]	DDC0_NCO_REGMAP_CHAN_SEL		NCO Channel Select Register Map Control.	0x0	R/W
				0000	Select NCO Channel 0.		
				0001	Select NCO Channel 1.		
				0010	Select NCO Channel 2.		
				0011	Select NCO Channel 3.		
				0100	Select NCO Channel 4.		

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
					…		
				1111	Select NCO Channel 15.		
0x633	DDC_PROFILE_CTRL	7	DDC0_PROFILE_UPDATE_MODE		DDC Profile Update Mode and DDC Phase Update Mode.	0x0	R/W
				0	Instantaneous/continuous update. Phase increment and phase offset values are updated immediately.		
				1	Phase increment and phase offset values are updated synchronously with the CHIP_TRANSFER bit is set low to high.		
		[6:4]	Reserved		Reserved.	0x0	R
		[3:0]	DDC0_PROFILE_UPDATE_INDEX		Profile Update Index. Indexes the NCO channel whose phase and offset is updated. The update method is based on the DDC_PHASE_UPDATE_MODE, which can be continuous or require a CHIP_TRANSFER.	0x0	R/W
				0000	Update NCO Channel 0.		
				0001	Update NCO Channel 1.		
				0010	Update NCO Channel 2.		
				0011	Update NCO Channel 3.		
				0100	Update NCO Channel 4.		
					…		
				1111	Update NCO Channel 15.		
0x634	DDC_PHASE_INC0	[7:0]	DDC0_PHASE_INC0		NCO Phase Increment Value, Bits [7:0]. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x635	DDC_PHASE_INC1	[7:0]	DDC0_PHASE_INC1		NCO Phase Increment Value, Bits [15:8]. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x636	DDC_PHASE_INC2	[7:0]	DDC0_PHASE_INC2		NCO Phase Increment Value, Bits[23:16]. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x637	DDC_PHASE_INC3	[7:0]	DDC0_PHASE_INC3		NCO Phase Increment Value, Bits[31:24]. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x638	DDC_PHASE_INC4	[7:0]	DDC0_PHASE_INC4		NCO Phase Increment Value, Bits[39:32]. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x639	DDC_PHASE_INC5	[7:0]	DDC0_PHASE_INC5		NCO Phase Increment Value, Bits[47:40]. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC_PHASE_INC × f_S)/2^{48}.	0x0	R/W
0x63A	DDC_PHASE_OFFSET0	[7:0]	DDC0_PHASE_OFFSET0		NCO Phase Offset Value, Bits[7:0]. Value in twos complement.	0x0	R/W
0x63B	DDC_PHASE_OFFSET1	[7:0]	DDC0_PHASE_OFFSET1		NCO Phase Offset Value, Bits[15:8]. Value in twos complement.	0x0	R/W
0x63C	DDC_PHASE_OFFSET2	[7:0]	DDC0_PHASE_OFFSET2		NCO Phase Offset Value, Bits[23:16]. Value in twos complement.	0x0	R/W
0x63D	DDC_PHASE_OFFSET3	[7:0]	DDC0_PHASE_OFFSET3		NCO Phase Offset Value, Bits[31:24]. Value in twos complement.	0x0	R/W
0x63E	DDC_PHASE_OFFSET4	[7:0]	DDC0_PHASE_OFFSET4		NCO Phase Offset Value, Bits[39:32]. Value in twos complement.	0x0	R/W
0x63F	DDC_PHASE_OFFSET5	[7:0]	DDC0_PHASE_OFFSET5		NCO Phase Offset Value, Bits[47:40]. Value in twos complement.	0x0	R/W
0x640	DDC_PHASE_INC_FRAC_A0	[7:0]	DDC0_PHASE_INC_FRAC_A0		Phase Increment Numerator, Bits[7:0]. Twos complement numerator correction term for modulus phase accumulator.	0x0	R/W
0x641	DDC_PHASE_INC_FRAC_A1	[7:0]	DDC0_PHASE_INC_FRAC_A1		Phase Increment Numerator, Bits[15:8]. Twos complement numerator correction term for modulus phase accumulator.	0x0	R/W

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x642	DDC_PHASE_INC_FRAC_A2	[7:0]	DDC0_PHASE_INC_FRAC_A2		Phase Increment Numerator, Bits [23:16]. Twos complement numerator correction term for modulus phase accumulator.	0x0	R/W
0x643	DDC_PHASE_INC_FRAC_A3	[7:0]	DDC0_PHASE_INC_FRAC_A3		Phase Increment Numerator, Bits [31:24]. Twos complement numerator correction term for modulus phase accumulator.	0x0	R/W
0x644	DDC_PHASE_INC_FRAC_A4	[7:0]	DDC0_PHASE_INC_FRAC_A4		Phase Increment Numerator, Bits [39:32]. Twos complement numerator correction term for modulus phase accumulator.	0x0	R/W
0x645	DDC_PHASE_INC_FRAC_A5	[7:0]	DDC0_PHASE_INC_FRAC_A5		Phase Increment Numerator, Bits [47:40] Twos complement numerator correction term for modulus phase accumulator.	0x0	R/W
0x646	DDC_PHASE_INC_FRAC_B0	[7:0]	DDC0_PHASE_INC_FRAC_B0		Phase Increment Denominator, Bits [7:0]. Twos complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x647	DDC_PHASE_INC_FRAC_B1	[7:0]	DDC0_PHASE_INC_FRAC_B1		Phase Increment Denominator, Bits [15:8]. Twos complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x648	DDC_PHASE_INC_FRAC_B2	[7:0]	DDC0_PHASE_INC_FRAC_B2		Phase Increment Denominator, Bits [23:16]. Twos complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x649	DDC_PHASE_INC_FRAC_B3	[7:0]	DDC0_PHASE_INC_FRAC_B3		Phase Increment Denominator, Bits [31:24]. Twos complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x64A	DDC_PHASE_INC_FRAC_B4	[7:0]	DDC0_PHASE_INC_FRAC_B4		Phase Increment Denominator, Bits [39:32]. Twos complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x64B	DDC_PHASE_INC_FRAC_B5	[7:0]	DDC0_PHASE_INC_FRAC_B5		Phase Increment Denominator, Bits [47:40]. Twos complement denominator correction term for modulus phase accumulator.	0x0	R/W
0x64C	DDC_TRANSFER_CTRL	[7:1]	Reserved		Reserved.	0x0	R
		0	DDC0_CHIP_TRANSFER		DDC Chip Transfer. Note that this bit updates the DDC phase increment and phase offset registers when DDC_PHASE_UPDATE_MODE = 1 and DDC_GPIO_CHIP_TRANSFER_MODE = 0.	0x0	R/W
				0	Do nothing.		
				1	Synchronizes data transfer from master registers to slave registers.		
0x64D	DDC_TRANSFER_STATUS	[7:1]	Reserved		Reserved.	0x0	R
		0	DDC0_CHIP_TRANSFER_STATUS		DDC Chip Transfer Status Bit.	0x0	R
				0	Data transfer from master register to slave register is complete.		
				1	Indicates the data transfer is not requested or not completed.		
0x650	MOD_NCO_PHASE_ERROR_LOAD_REG0	[7:0]	MOD_NCO_PHASE_ERROR_LOAD_VALUE[7:0]		MOD NCO Phase Error Value.	0x0	R/W
0x651	MOD_NCO_PHASE_ERROR_LOAD_REG1	[7:0]	MOD_NCO_PHASE_ERROR_LOAD_VALUE[15:8]		MOD NCO Phase Error Value.	0x0	R/W
0x652	MOD_NCO_PHASE_ERROR_LOAD_REG2	[7:0]	MOD_NCO_PHASE_ERROR_LOAD_VALUE[23:16]		MOD NCO Phase Error Value.	0x0	R/W
0x653	MOD_NCO_PHASE_ERROR_LOAD_REG3	[7:0]	MOD_NCO_PHASE_ERROR_LOAD_VALUE[31:24]		MOD NCO Phase Error Value.	0x0	R/W
0x654	MOD_NCO_PHASE_ERROR_LOAD_REG4	[7:0]	MOD_NCO_PHASE_ERROR_LOAD_VALUE[39:32]		MOD NCO Phase Error Value.	0x0	R/W
0x655	MOD_NCO_PHASE_ERROR_LOAD_REG5	[7:0]	MOD_NCO_PHASE_ERROR_LOAD_VALUE[47:40]		MOD NCO Phase Error Value.	0x0	R/W

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x656	MOD_NCO_PHASE_ ERROR_LOAD_CTRL	[7:1]	Reserved		Reserved.	0x0	R
		0	MOD_NCO_PHASE_ ERROR_LOAD_ENABLE		MOD NCO Phase Error Load Enable.	0x0	R/W
0x657	MOD_NCO_PHASE_ ERROR_LOAD_STATUS	[7:3]	Reserved		Reserved.	0x0	R
		2	MOD_NCO_PHASE_ ERROR_LOAD_STATUS		MOD NCO Phase Error Load Status.	0x0	R
		[1:0]	Reserved		Reserved.	0x0	R
0x65F	DDC_PSW_0	[7:0]	DDC0_PSW0		DDC Profile Select Word. (PSW), Bits[7:0]. The PSW specifies the rollover point for the profile select timer (PST) in encode samples. The channel selection counter increments when the PST rolls over to zero, and channel selection occurs through the PST.	0x0	R/W
0x660	DDC_PSW_1	[7:0]	DDC0_PSW1		DDC PSW, Bits[15:8]. The PSW specifies the rollover point for the PST in encode samples. The channel selection counter increments when the PST rolls over to zero, and channel selection occurs through the PST.	0x0	R/W
0x661	DDC_PSW_2	[7:0]	DDC0_PSW2		DDC PSW, Bits[23:16]. The PSW specifies the rollover point for the PST in encode samples. The channel selection counter increments when the PST rolls over to zero, and channel selection occurs through the PST.	0x0	R/W
0x662	DDC_PSW_3	[7:0]	DDC0_PSW3		DDC PSW, Bits[31:24]. The PSW specifies the rollover point for the PST in encode samples. The channel selection counter increments when the PST rolls over to zero, and channel selection occurs through the PST.	0x0	R/W
0x663	DDC_PSW_4	[7:0]	DDC0_PSW4		DDC PSW, Bits[39:23]. The PSW specifies the rollover point for the PST in encode samples. The channel selection counter increments when the PST rolls over to zero, and channel selection occurs through the PST.	0x0	R/W
0x664	DDC_PSW_5	[7:0]	DDC0_PSW5		DDC PSW, Bits[47:40]. The PSW specifies the rollover point for the PST in encode samples. The channel selection counter increments when the PST rolls over to zero, and channel selection occurs through the PST.	0x0	R/W
0x665	DDC_ACTIVE_PHASE_ INC0	[7:0]	DDC0_ACTIVE_PHASE_ INC0		NCO Active Phase Increment Value, Bits[7:0].	0x0	R
0x666	DDC_ACTIVE_PHASE_ INC1	[7:0]	DDC0_ACTIVE_PHASE_ INC1		NCO Active Phase Increment Value, Bits[15:8].	0x0	R
0x667	DDC_ACTIVE_PHASE_ INC2	[7:0]	DDC0_ACTIVE_PHASE_ INC2		NCO Active Phase Increment Value, Bits[23:16].	0x0	R
0x668	DDC_ACTIVE_PHASE_ INC3	[7:0]	DDC0_ACTIVE_PHASE_ INC3		NCO Active Phase Increment Value, Bits[31:24].	0x0	R
0x669	DDC_ACTIVE_PHASE_ INC4	[7:0]	DDC0_ACTIVE_PHASE_ INC4		NCO Active Phase Increment Value, Bits[39:32].	0x0	R
0x66A	DDC_ACTIVE_PHASE_ INC5	[7:0]	DDC0_ACTIVE_PHASE_ INC5		NCO Active Phase Increment Value, Bits[47:40].	0x0	R
0x66B	DDC_ACTIVE_PHASE_ OFFSET0	[7:0]	DDC0_ACTIVE_PHASE_ OFFSET0		NCO Active Phase Increment Value, Bits[7:0].	0x0	R
0x66C	DDC_ACTIVE_PHASE_ OFFSET1	[7:0]	DDC0_ACTIVE_PHASE_ OFFSET1		NCO Active Phase Increment Value, Bits[15:8].	0x0	R
0x66D	DDC_ACTIVE_PHASE_ OFFSET2	[7:0]	DDC0_ACTIVE_PHASE_ OFFSET2		NCO Active Phase Increment Value, Bits[23:16].	0x0	R
0x66E	DDC_ACTIVE_PHASE_ OFFSET3	[7:0]	DDC0_ACTIVE_PHASE_ OFFSET3		NCO Active Phase Increment Value, Bits[31:24].	0x0	R
0x66F	DDC_ACTIVE_PHASE_ OFFSET4	[7:0]	DDC0_ACTIVE_PHASE_ OFFSET4		NCO Active Phase Increment Value, Bits[39:32].	0x0	R
0x670	DDC_ACTIVE_PHASE_ OFFSET5	[7:0]	DDC0_ACTIVE_PHASE_ OFFSET5		NCO Active Phase Increment Value, Bits[47:40].	0x0	R

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x671	TIMESTAMP_READ_CTRL	[7:1]	Reserved		Reserved.	0x0	R
		0	TIMESTAMP_READ_ENABLE		Timestamp Read Enable. Rising edge on time stamp read enable is detected and then timestamp counter data is latched. This stored time stamp data is used for timestamp status read.	0x0	R/W
0x672	TIMESTAMP_COUNTER_REG0	[7:0]	TIMESTAMP[7:0]		Time Stamp Counter Value, Bits[7:0].	0x0	R
0x673	TIMESTAMP_COUNTER_REG1	[7:0]	TIMESTAMP[15:8]		Time Stamp Counter Value, Bits[15:8].	0x0	R
0x674	TIMESTAMP_COUNTER_REG2	[7:0]	TIMESTAMP[23:16]		Time Stamp Counter Value, Bits[23:16].	0x0	R
0x675	TIMESTAMP_COUNTER_REG3	[7:0]	TIMESTAMP[31:24]		Time Stamp Counter Value, Bits[31:24].	0x0	R
0x676	TIMESTAMP_COUNTER_REG4	[7:0]	TIMESTAMP[39:32]		Time Stamp Counter Value, Bits[39:32].	0x0	R
0x677	TIMESTAMP_COUNTER_REG5	[7:0]	TIMESTAMP[47:40]		Time Stamp Counter Value, Bits[47:40].	0x0	R
0x678	TIMESTAMP_COUNTER_REG6	[7:0]	TIMESTAMP[55:48]		Time Stamp Counter Value, Bits[55:48].	0x0	R
0x679	TIMESTAMP_COUNTER_REG7	[7:0]	TIMESTAMP[63:56]		Time Stamp Counter Value, Bits[63:56].	0x0	R
0x681	JTX_CLK	[7:5]	Reserved		Reserved.	0x0	R
		4	JTX_CLK_EN		JTx Clock Enable Selection.	0x0	R/W
				0	DDC and JTx clocks disabled.		
				1	DDC and JTx clocks enabled.		
		[3:0]	Reserved		Reserved.	0x0	R
0x690	SYSREF_DELAY	[7:0]	SYSREF_PROGDELAY		Programmable Delay on SYSREF_x Path to DDC NCO. 8-bit delay in terms of sampling clock.	0x0	R/W
0x691	TRIG_DELAY	[7:0]	TRIG_PROGDELAY		Programmable Delay on TRIG_x Path to DDC NCO. 8-bit delay in terms of sampling clock.	0x0	R/W
0x692	TIMESTAMP_DELAY	[7:0]	TIMESTAMP_PROGDELAY		Programmable Delay on Time Stamp Path in DFORMAT. 8-bit delay in terms of sampling clock.	0x0	R/W
0x693	SYSREF_RESYNC	[7:1]	Reserved		Reserved.	0x0	R
		0	SYSREF_RESYNC		SYSREF_x Resynchronization Mode Enable. SYSREF_x timestamp mode is for Subclass 0 operation. All Subclass 1 operation for deterministic latency must set to Bit 0 = 1 (SYSREF_x resynchronization mode enabled).	0x0	R/W
				0	SYSREF_x timestamp mode enabled.		
				1	SYSREF_x resynchronization mode enabled.		
0x1507	RESET_CTRL	[7:5]	Reserved		Reserved.	0x2	R
		4	RESET_JTX		Reset JTx Block.	0x0	R/W
		3	Reserved		Reserved.	0x0	R/W
		2	RESET_DPATH		Reset Datapath. Apply to main digital.	0x0	R/W
		1	RESET_DIG_ANA		Reset Digital Blocks and Registers in the Analog Section.	0x0	R/W
		0	RESET_ANA		Reset Analog Section.	0x0	R/W
0x1508	SYSREF_CTRL	[7:2]	Reserved		Reserved.	0x0	R
		1	SYSREF_TRANSITION_SEL		SYSREF_x Transition Selection.	0x0	R/W
				0	SYSREF_x is valid on low to high transitions using selected CLK_x edge.		
				1	SYSREF is valid on high to low transitions using selected CLK_x edge.		
		0	SYSREF_EDGE_SEL		SYSREF_x Capture Edge Selection.	0x0	R/W
				0	Captured on rising edge of CLK_x input.		
				1	Captured on falling edge of CLK_x input.		
0x1509	SYSREF_STATUS	[7:4]	SYSREF_HOLD_STATUS		Gives Status of Hold Capture Window.	0xF	R
		[3:0]	SYSREF_SETUP_STATUS		Gives Status of Setup Capture Window.	0x8	R

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x150A	LVDS_SEL	[7:2]	Reserved		Reserved.	0x0	R
		1	TRIG_RX_LVDS_SEL		Switch Between LVDS and Differential CMOS Input Modes for TRIG_x.	0x0	R/W
				0	Differential CMOS selected.		
				1	LVDS selected.		
		0	SYSREF_RX_LVDS_SEL		Switch between LVDS and Differential CMOS Input Modes for SYSREF_x.	0x0	R/W
				0	Differential CMOS selected		
				1	LVDS selected		
0x150C	SPI_EN_DCS	[7:1]	Reserved		Reserved.	0x0	R
		0	SPI_EN_DCS		Duty Cycle Stabilizer.	0x0	R/W
				0	Disable.		
				1	Enable.		
0x150D	SPI_EN_FDLY	[7:2]	Reserved		Reserved.	0x0	R
		1	SPI_EN_SFDLY		Super Fine Delay Cell enable bit.	0x0	R/W
				0	Disabled.		
				1	Enabled (along with half fine delay cell).		
		0	SPI_EN_FDLY		Fine Delay Cell Enable Bit. Two halves fine delay cells in series. Each has 24 steps adjustments.	0x0	R/W
				0	Disabled.		
				1	Enabled (two halves fine delay cells).		
0x150E	SPI_TRM_FINE_DLY	[7:0]	SPI_TRM_FINE_DLY		Clock Fine Adjustment. This is an unsigned control to adjust sampling clock skew in 1.1 ps per step with 48 total steps. These bits are used only when Register 0x150D, Bit 1 or Bit 0 are set to 1. Minimum delay = 0, maximum delay = 48.	0x0	R/W
0x150F	SPI_TRM_SUPER_FINE_DLY	[7:0]	SPI_TRM_SUPER_FINE_DLY		Clock Super Fine Delay Adjustment. This is an unsigned control to adjust sampling clock skew in 16 f_S/step with 255 total steps. These bits are only used when Register 0x150D, Bit 1 = 1, Register 0x1510, Bit 0 = 0. Minimum delay = 0, maximum delay = 255.	0x0	R/W
0x1510	SPI_SFDC_BYPASS	[7:1]	Reserved		Reserved.	0x0	R
		0	SPI_SFDC_BYPASS		Super Fine Delay Cell Bypassed. This bit works in conjunction with SPI_EN_SFDLY bit. When SPI_EN_SFDLY = 0, SPI_SFDC_BYPASS = 0 or 1 (don't care). When SPI_EN_SFDLY = 1, SPI_SFDC_BYPASS = 1 super fine delay cell bypassed.	0x0	R/W
0x1511	BKEND_TOP_GAIN_ADJ	[7:1]	Reserved		Reserved.	0x0	R
		0	GAIN_2X		Setting this Bit to 1 Doubles the Data at the Output.	0x0	R/W
0x1512	SUPPLY_MON1	[7:6]	Reserved		Reserved.	0x0	R
		5	SUPMON_VTTPHY_SER_0P9		1 V Supply Monitor for SERDES.	0x1	R
		4	SUPMON_VDDSYNTH_LCPLL_0P9		1 V Supply Monitor for JESD204B Synthesizer.	0x1	R
		3	SUPMON_VDDD_LCPLL_0P9		1 V Digital Supply Monitor for JESD PLL.	0x1	R
		2	SUPMON_VDDA_REFADC_1P0		1 V Analog Supply Monitor for Reference ADC.	0x1	R
		1	SUPMON_VDDA_CLK_1P0		1 V Analog Supply Monitor for Clock.	0x1	R
		0	SUPMON_VDDA_1P0		1 V Analog Supply Monitor.	0x1	R
0x1513	SUPPLY_MON2	[7:5]	Reserved		Reserved.	0x0	R
		4	SUPMON_VDDA_TMU_1P8		2 V Analog Supply Monitor for TMU.	0x1	R
		3	SUPMON_VDDLDO_LCPLL_1P8		2 V Supply Monitor for JESD204B LDO.	0x1	R

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
		2	SUPMON_VDDD_SPI_1P8		2 V Digital Supply Monitor for SPI Pads.	0x1	R
		1	SUPMON_VDDA_REF_2P0		2 V Analog Supply Monitor for Reference.	0x1	R
		0	SUPMON_VDDA_BUF_2P0		2 V Analog Supply Monitor for Buffer	0x1	R
0x1514	SUPPLY_MON3	[7:2]	Reserved		Reserved.	0x0	R
		1	SUPMON_VEEA_NEG1P0		−1 V Analog Supply Monitor.	0x1	R
		0	SUPMON_VEEA_BUF_NEG1P0		−1 V Analog Supply Monitor for Buffer.	0x1	R
0x1515	PDOWN_CTRL	[7:3]	PDB_REF_NOHCLK		Power-Down for Reference.	0x1F	R/W
		2	SPI_PDB_CLKBUF		Power-Down for Clock Buffer.	0x1	R/W
		1	STDBY_CHIP		Standby Chip.	0x0	R/W
		0	PD_CHIP		Power Down Chip.	0x0	R/W
0x1516	SPI_EN_FDLY_SYS	[7:2]	Reserved		Reserved.	0x0	R
		1	SPI_EN_SFDLY_SYS		Super Fine Delay Cell Enable Bit for System Clock.	0x0	R/W
				0	Disabled.		
				1	Enabled (along with half fine delay cell).		
		0	SPI_EN_FDLY_SYS		Fine Delay Cell enable Bit for System Clock. Two halves fine delay cells in series. Each has 24 steps adjustments.	0x0	R/W
				0	Disabled.		
				1	Enabled (two halves fine delay cells).		
0x1517	SPI_TRM_FINE_DLY_SYS	[7:0]	SPI_TRM_FINE_DLY_SYS		Clock Fine Adjustment for System Clock. This is an unsigned control to adjust the system clock skew in 1.1 ps per step with 48 total steps. These bits are used only when Register 0x1516, Bit 1 or Bit 0 are set to 1. Minimum delay = 0, maximum delay = 48.	0x0	R/W
0x1518	SPI_TRM_SUPER_FINE_DLY_SYS	[7:0]	SPI_TRM_SUPER_FINE_DLY_SYS		Clock super fine delay SYS clock adjustment. This is an unsigned control to adjust the system clock skew in 16 f_S/step with 255 total steps. These bits are only used when Register 0x1516, Bit 1 = 1, Register 0x1519, Bit 0 = 0. Minimum delay = 0, maximum delay = 255.	0x0	R/W
0x1519	SPI_SFDC_BYPASS_SYS	[7:1]	Reserved		Reserved.	0x0	R
		0	SPI_SFDC_BYPASS_SYS		Super Fine Delay Cell Bypassed for the system clock. This bit works in conjunction with the SPI_EN_SFDLY_SYS bit. When SPI_EN_SFDLY_SYS = 0, SPI_SFDC_BYPASS_SYS = 0 or 1 (don't care). When SPI_EN_SFDLY_SYS = 1, SPI_SFDC_BYPASS_SYS = 1 super fine delay cell bypassed for the system clock.	0x0	R/W
0x151A	EN_VCM_MODE	[7:2]	Reserved		Reserved.	0x0	R
		[1:0]	EN_VCM_MODE		VCM Enable Mode Control.	0x1	R/W
				00	Internal and External VCM control buffers disabled.		
				01	Startup. Internal VCM control buffer enabled.		
				10	External VCM control buffer enabled.		
				11	Internal and External VCM control buffers enabled. Auxiliary mode.		

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x151B	SPI_NVG1	[7:3]	Reserved		Reserved.	0x0	R
		[2:1]	SPI_EN_SUM_NVG_1P0		There are several NVG loops that control the enabled loops enabled, which can improve the efficiency at nominal mode. When input buffer is at high performance mode, the binary value is 11, and at nominal mode, it is 10.	0x2	R/W
		0	SPI_EN_NVG_1P0		Negative 1 V Generator Enable Bit.	0x1	R/W
				0	Power down.		
				1	Enable.		
0x151D	CLOCK_DETECT_CTRL	[7:2]	Reserved		Reserved.	0x0	R
		1	CLOCK_DETECT_DIS_FLAG		Disable Clock Detect Function as a Halt.	0x1	R/W
				0	Enabled.		
				1	Disabled.		
		0	CLOCK_DETECT		Status of Clock Detect Locked. This bit indicates the instantaneous value of the clock detect circuit.	0x1	R
				0	Out of lock.		
				1	In lock.		
0x151E	MCS_CTRL	[7:4]	Reserved		Reserved.	0x0	R
		[3:2]	MCS_TRIG_FREQ_HOP_MODE		TRIG_x for Frequency Hopping or Enable When SYSREF_OUT/div8 Counter Used to Frequency Hop.	0x0	R/W
				00	Disable.		
				01	EDGE_TRIGGERED. The rising edge of the TRIG_x pin causes a frequency hop on the NCO. This mode only requires the TRIG_x buffer to be enabled.		
		1	MCS_DTLL_LOCK_DETECT		MCS Lock Status for Continuous SYSREF_x Modes. Asserted when lock is achieved.	0x0	R
		0	Reserved		Reserved.	0x0	R/W
0x1521	MCS_SYSREF_IGNORE_COUNT	[7:0]	MCS_SYSREF_IGNORE_COUNT		Number of SYSREF_x Pulses to Ignore at Startup.	0x0	R/W
0x1523	GPIO_PDEB	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	GPIO_PDEB		GPIO Pull Down Active Low.	0x1F	R/W
0x1600	USER_CTRL_TRANSFER	[7:1]	Reserved		Reserved.	0x0	R
		0	USER_CTRL_TRANSFER		Use Control Transfer Bit. If set to 1, apply latest settings for Register 0x1601 to Register 0x1636. Self clearing.	0x0	R/W
0x1601	CAL_CONTROL	[7:1]	Reserved		Reserved.	0x0	R
		0	CAL_FREEZE		Freeze Bit to Halt Background Calibrations.	0x0	R/W
0x1602	CLOCK_RATE	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	CLOCK_RATE		User to Specify Operating Clock Rate for Calibration Adaptation. Support for up to four clock rates (user selectable).	0x0	R/W
				0	Clock Rate 0.		
				1	Clock Rate 1.		
				10	Clock Rate 2.		
				11	Clock Rate 3.		
0x1606	GPIO_CONTROL	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	GPIO_PROFILE		Define GPIO Profile to Use.	0x0	R/W
				0	Disabled. GPIO profiles disabled.		
				1	GPIO[4] = FREEZE_CAL GPIO[3:0] = Profile[3:0]		
				10	FREEZE_CAL disabled GPIO[3:0] = Profile[3:0]		
0x1609	MAX_TEMPERATURE_LSB	[7:0]	MAX_TEMPERATURE[7:0]		Maximum Temperature of All Temperature Sensors. Q9.7 format. See TMU section.	0x0	R
0x160A	MAX_TEMPERATURE_MSB	[7:0]	MAX_TEMPERATURE[15:8]		Maximum Temperature of All Temperature Sensors. Q9.7 format.	0x0	R

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x160D	MIN_TEMPERATURE_LSB	[7:0]	MIN_TEMPERATURE[7:0]		Minimum Temperature of all Temperature Sensors. Q9.7 format. See TMU section.	0x0	R
0x160E	MIN_TEMPERATURE_MSB	[7:0]	MIN_TEMPERATURE[15:8]		Minimum Temperature of all Temperature Sensors. Q9.7 format. See TMU section.	0x0	R
0x160F	FD_OV_CONTROL	[7:2]	Reserved		Reserved.	0x0	R
		1	OV_EN		Over Voltage FD Pin Enable.	0x0	R/W
		0	FD_EN		Fast Detect FD Pin Enable.	0x0	R/W
0x1612	CHANNEL_GAIN_ CONTROL_LSB	[7:0]	CHANNEL_GAIN_ CONTROL[7:0]		Gain Adjustment Control for Entire Channel. Value is represented as Q2.14 format.	0x0	R/W
0x1613	CHANNEL_GAIN_ CONTROL_MSB	[7:0]	CHANNEL_GAIN_ CONTROL[15:8]		Gain Adjustment Control for Entire Channel. Value is represented as Q2.14 format.	0x40	R/W
0x1614	ENCODE_CHANGE (only for changing sampling rate on the fly)	[7:3]	Reserved		Reserved.	0x0	R
		2	ACK_ENCODE_CHANGE_ DONE		Acknowledge Encode Change Complete.	0x0	R
		1	ENCODE_CHANGE_ DONE		Encode Clock Rate is Changed Indication Bit. Set by user.	0x0	R/W
		0	READY_FOR_ENCODE_ CHANGE		Change Encode Clock Rate Permitted Bit. Indicated by user.	0x0	R
0x1615	VREF_IMPORT_EN	[7:1]	Reserved		Reserved.	0x0	R
		0	VREF_IMPORT_EN		Enable Import of External Bandgap Voltage.	0x0	R/W
0x1616	VREF_MON_SEL	[7:0]	VREF_MON_SEL		Import External Bandgap Voltage (VREF_IMPORT_EN = 1).	0x0	R/W
				1	Import VREF.		
0x1617	DC_COUPLED_MODE_EN	[7:1]	Reserved		Reserved.	0x0	R
		0	DC_COUPLED_MODE_EN		Enable to Retain DC Content of Input Signal.	0x0	R/W
				0	AC-coupled mode. Actively null dc content of input signal.		
				1	DC-coupled mode. Retain dc content of input signal.		
0x1621	MCS_MODE	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	MCS_MODE		MCS Modes.	0x0	R/W
				1	Sampled SYSREF_x input with setup/hold time information.		
				1001	Averaged SYSREF_x mode.		
0x1622	MCS_CTRL	[7:2]	Reserved		Reserved.	0x0	R
		1	MCS_LOCK_EN		Enable MCS to Lock to Internal SYSREF_x.	0x0	R/W
				0	No action.		
				1	Lock once (foreground locking).		
		0	Reserved		Reserved	0x0	R/W
0x1623	MCS_CALC_TIME_DIFF1	[7:0]	CALC_TIME_DIFF[7:0]		Calculated Time Difference Between Input SYSREF_x and Local SYSREF, Bits[7:0]. Format is 24.8, expressed in picoseconds with a range of ±8.39 ms and a resolution of 3.9 fs.	0x0	R/W
0x1624	MCS_CALC_TIME_DIFF2	[7:0]	CALC_TIME_DIFF[15:8]		Calculated Time Difference Between Input SYSREF_x and Local SYSREF, Bits[15:8]. Format is 24.8, expressed in picoseconds with a range of ±8.39 ms and a resolution of 3.9 fs.	0x0	R/W
0x1625	MCS_CALC_TIME_DIFF3	[7:0]	CALC_TIME_DIFF[23:16]		Calculated Time Difference Between Input SYSREF_x and Local SYSREF, Bits[23:16]. Format is 24.8, expressed in picoseconds with a range of ±8.39 ms and a resolution of 3.9 fs.	0x0	R/W
0x1626	MCS_CALC_TIME_DIFF4	[7:0]	CALC_TIME_DIFF[31:24]		Calculated Time Difference Between Input SYSREF_x and Local SYSREF, Bits[31:24]. Format is 24.8, expressed in picoseconds with a range of ±8.39 ms and a resolution of 3.9 fs.	0x0	R/W

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x1627	MCS_KNOWN_SYSREF_ PERIOD1	[7:0]	KNOWN_SYSREF_ PERIOD[7:0]		Period of Input SYSREF_x, Bits[7:0]. Expressed as an integer multiple of eight (of the encode clock period). This register provides the device with the average SYSREF_x rate is in the system, which generates the local, internal SYSREF_x. This value is expressed as units of the sample clock divided by eight. Therefore, the SYSREF_x period is SAMPLE_CLOCK_FREQ/ (8 × KNOWN_SYSREF_PERIOD).	0x0	R/W
0x1628	MCS_KNOWN_SYSREF_ PERIOD2	[7:0]	KNOWN_SYSREF_ PERIOD[15:8]		Period of Input SYSREF_x, Bits[15:8]. Expressed as an integer multiple of eight (of the encode clock period). This register provides the device with the average SYSREF_x rate is in the system, which generates the local, internal SYSREF_x. This value is expressed as units of the sample clock divided by eight. Therefore, the SYSREF_x period is SAMPLE_CLOCK_FREQ/ (8 × KNOWN_SYSREF_PERIOD).	0x0	R/W
0x1629	MCS_KNOWN_SYSREF_ PERIOD3	[7:0]	KNOWN_SYSREF_ PERIOD[23:16]		Period of Input SYSREF_x, Bits[23:16]. Expressed as an integer multiple of eight (of the encode clock period). This register provides the device with the average SYSREF_x rate is in the system, which generates the local, internal SYSREF_x. This value is expressed as units of the sample clock divided by eight. Therefore, the SYSREF_x period is SAMPLE_ CLOCK_FREQ/(8 × KNOWN_SYSREF_PERIOD).	0x0	R/W
0x162A	MCS_SYSREF_AVGING_ COUNT1	[7:0]	MCS_SYSREF_AVGING_ COUNT[7:0]		Number of SYSREF_x Pulses to Average, Bits[7:0]. Actual number is (N + 1) × 16 SYSREF_x per iterations. Multiple such iterations are required to achieve a lock state. Averaging the noise from the TDC reduces jitter on the SYSREF_x inputs. The noise of the TDC is approximately 90 ps rms and by averaging P samples the noise is reduced by SQRT(P). By setting this to 999, 16,000 SYSREF_x samples are averaged bring the noise to approximately 711 fs rms.	0x0	R/W
0x162B	MCS_SYSREF_AVGING_ COUNT2	[7:0]	MCS_SYSREF_AVGING_ COUNT[15:8]		Number of SYSREF_x Pulses to Average, Bits[15:8]. Actual number is (N + 1) × 16 SYSREF_x per iterations. Multiple such iterations are required to achieve a lock state. Averaging the noise from the TDC reduces jitter on the SYSREF_x inputs. The noise of the TDC is approximately 90 ps rms and by averaging P samples the noise is reduced by SQRT(P). By setting this to 999, 16,000 SYSREF_x samples are averaged bring the noise to approximately 711 fs rms.	0x0	R/W
0x162D	MCS_SAMPLE_CLK_ PERIOD1	[7:0]	SAMPLE_CLOCK_ PERIOD[7:0]		Period of Sample Clock, Bits[7:0]. This value is in 16'16 format, expressed in picoseconds with a range of 65.5 ns and a resolution of 0.015 fs. This is the known period of the sample clock in the user application. This number is a reference so that the MCS_CALC_ TIME_DIFF value can be expressed to the user as a true time domain measurement.	0x0	R/W
0x162E	MCS_SAMPLE_CLK_ PERIOD2	[7:0]	SAMPLE_CLOCK_ PERIOD[15:8]		Period of Sample Clock, Bits[15:8]. This value is in 16'16 format, expressed in picoseconds with a range of 65.5 ns and a resolution of 0.015 fs. This is the known period of the sample clock in the user application. This number is a reference so that the MCS_CALC_ TIME_DIFF value can be expressed to the user as a true time domain measurement.	0x0	R/W

Address	Register Name	Bits	Bit Name	Settings	Description	Default	Access
0x162F	MCS_SAMPLE_CLK_PERIOD3	[7:0]	SAMPLE_CLOCK_PERIOD[23:16]		Period of Sample Clock, Bits[23:16]. This value is in 16'16 format, expressed in picoseconds with a range of 65.5 ns and a resolution of 0.015 fs. This is the known period of the sample clock in the user application. This number is a reference so that the MCS_CALC_TIME_DIFF value can be expressed to the user as a true time domain measurement.	0x0	R/W
0x1630	MCS_SAMPLE_CLK_PERIOD4	[7:0]	SAMPLE_CLOCK_PERIOD[31:24]		Period of Sample Clock, Bits[31:24]. This value is in 16'16 format, expressed in picoseconds with a range of 65.5 ns and a resolution of 0.015 fs. This is the known period of the sample clock in the user application. This number is a reference so that the MCS_CALC_TIME_DIFF value can be expressed to the user as a true time domain measurement.	0x0	R/W
0x1636	MCS_PHASE_SLIP_MODE	[7:1]	Reserved		Reserved.	0x0	R
		0	MCS_PHASE_SLIP_MODE		MCS Phase Slip Mode Bit. When this bit is set to 0, the synchronization accuracy is limited to eight sample clocks and an internal divide by 8 clock divider is used to drive the local SYSREF counter. When this bit is set to 0, the phase of this divider is not modified, and the accuracy of the synchronization is only within 8 sample clocks. When this bit is set to 1, the phase of the divider is modified so that synchronization within a single sample clock cycle can be achieved.	0x0	R/W

APPLICATIONS INFORMATION

The following sections contain procedures necessary to properly operate the AD9213 within a given application.

STARTUP SEQUENCE

To start the device, take the following steps:

1. Power up the AD9213. There is no supply sequencing requirement. The sample clock can be applied after power is applied. The sample clock must be applied before the write to Register 0x26 = 0x08 (see Step 5).
2. Assert a Pin Reset. Take the AD9213 RSTB pin from high (SVDD2 voltage) to low (0 V), then back to high (SVDD2 voltage).
3. Write Register 0x0 = 0x24 to set the SPI address ascension mode to increment.
4. Wait 100 ms before performing the next step.
5. Write Register 0x26 = 0x08 to configure the AD9213 to receive sample clock signal. Sample clock must be applied before this step is performed.
6. Wait 100 ms before performing the next step.
7. Perform the user specific configuration of DDC, NCO, and JESD, which varies depending on the required application.

   This example is for 16 lane, M = 2, complex decimate by 8, N = N' = 16, with no NCO configuration.
   a) Write Register 0x504, Bit 4 = 1. Set SYNC pin logic type: 0 = CMOS, 1 = LVDS.
   b) Write Register 0x520 = 0x8F. Scrambler on, L = 16 lanes.
   c) Write Register 0x521 = 0x01. Set F = 2.
   d) Write Register 0x522 = 0x1F. K = 32 (default).
   e) Write Register 0x523 = 0x01. M = 2 (2 virtual converters, I/Q).
   f) Write Register 0x524 = 0xCF. Set N = 16.
   g) Write Register 0x525 = 0x0F. N' = 16, Subclass 0 operation.
   h) Write Register 0x606 = 0x01. Complex decimation enabled.
   i) Write Register 0x607 = 0x03. Chip decimate by 8
   j) Write Register 0x630 = 0x00. Bit 4 = 0. Complex output, Bits[3:2] = 0 NCO enabled (at 0 Hz), Bit 1 = 0 DDC 0 dB gain.
   k) Write Register 0x631 = 0x02. DDC decimate by 8.
8. Write Register 0x681 = 0x10. Enables DDC and JTX clocks.
9. Write Register 0x570, Bit 0 = 0, powers down JESD204B PLL
10. Write Register 0x570, Bit 0 = 1. powers up JESD204B PLL
11. Read Register 0x501. Confirm if JESD204B PLL is locked, Bit 7 = 1 indicates lock.

CHANGING SAMPLE CLOCK FREQUENCY WITHOUT POWER DOWN

To change the sample clock frequency (encode clock rate) without powering-down the ADC, take the following steps:

1. Write Register 0x332 = 0x02 to alert the AD9213 that the user is changing the clock frequency.
2. Read Register 0x1614, Bit 0. Wait for this bit to go high, which indicates that the user can change the encode clock rate.
3. Write Register 0x1602 = 0x01. This selects the coefficient location for Clock Rate 1.
4. Change the frequency of the clock applied to the CLK_P and CLK_N pins.
   a. Change any other necessary parameters due to the clock frequency change. For example, JESD PLL divider settings related to clock rate changes.
5. Write Register 0x1614, Bit 1 = 1. This notifies the AD9213 that the sample clock frequency has been changed.
6. Read Register 0x1614, Bit 2. Wait for this bit to go high which indicates that the change is complete.

The AD9213 now functions at the new sample frequency.

The coefficients from Register 0x1602 = 0x01 are now for the new, user selected clock frequency. At this point, coefficients are stored for two clock frequencies: Register 0x1602 = 0x00, coefficients for Clock Rate 0 (the original sample rate), and Register 0x1602 = 0x01, coefficients for Clock Rate 1 (the new sample rate).

To return to the original sample rate (Clock Rate 0), perform the procedure outlined in this section and set the Register 0x1602 clock rate parameter to Clock Rate 0.

The AD9213 now functions at the selected sample frequency, and the ADC is ready for operation at Clock Rate 0 within a few microseconds.

The procedure described in this section can be performed for four sample clock frequencies, including the original frequency used by the AD9213 at power-up. The coefficients for different clock frequencies are accessed by the different writes to Register 0x1602.

The following are examples of write operations to access the coefficients for various clock frequencies:

- Write Register 0x1602 = 0x00. This is the default value and contains coefficients for the original sample clock frequency (Clock Rate 0).
- Write Register 0x1602 = 0x01. This is points to Clock Rate 1 and contains coefficients for the user selected clock frequency (Clock Rate 1).
- Write Register 0x1602 = 0x02. This is points to Clock Rate 2 and contains coefficients for the user selected clock frequency (Clock Rate 2).

- Write Register 0x1602 = 0x03. This is points to Clock Rate 3 and contains coefficients for the user selected clock frequency (Clock Rate 3).

The coefficients for 10 GSPS are initially stored in all four locations by default.

The first time a sample clock frequency is used, a few seconds are required for the coefficients to converge and store as Clock Rate 0, Clock Rate 1, Clock Rate 2, or Clock Rate 3. In the next instance a specific clock rate is used with its associated set of stored coefficients, only a few microseconds are required to make the change. Note that additional time is required for the device to perform the SPI writes described in this section.

This procedure must be performed from the beginning if the AD9213 is powered down.

POWER SUPPLY RECOMMENDATIONS

Several of the AD9213 supply domains can be combined and powered by the supply configuration shown in Figure 126 if desired. This is an example configuration for minimizing power supply components and power domains. This approach can slightly increase the risk of switching regulator artifacts being injected into the power supply domains of the ADC. Initial evaluations using this configuration suggest the noise impact is minimal and is typically outweighed by its simplicity and use of fewer power supply components. Use of linear regulators and isolating specific supply pins can result in less noise.

An effective way to add power supply bypass capacitance to the AD9213 PCB is to use through vias on the AD9213 BGA power pads. Use 0201 (0603 Metric), 0.1 µF surface mount capacitors directly below the BGA footprint on the opposite side of the board, connecting the supply pins to the adjacent ground pins. Surface mount solder pads are required to accommodate the capacitors.

All ground pins can be connected to the same planes and combined into one domain at the board level

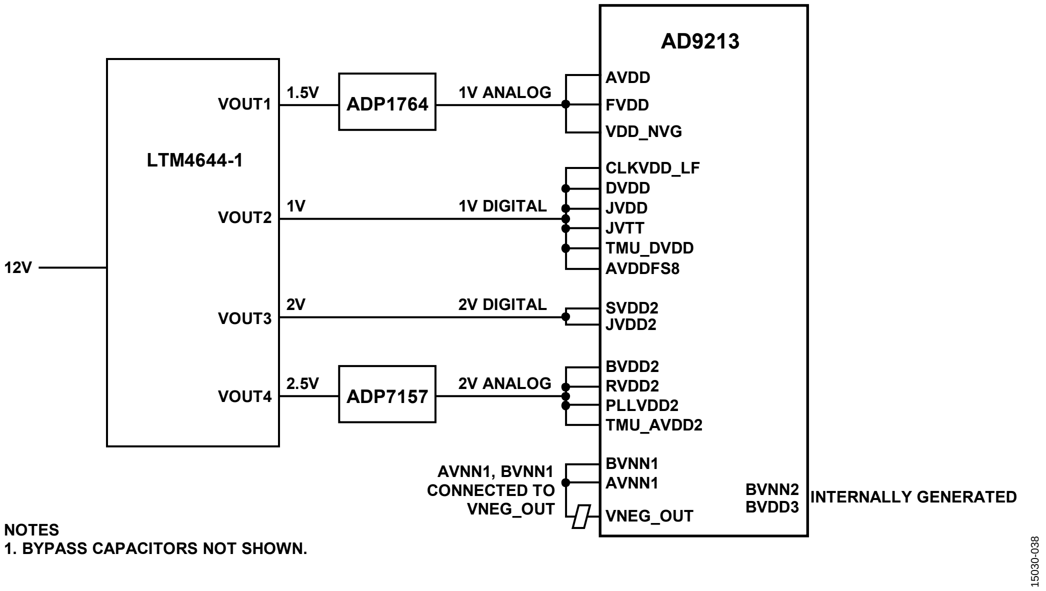


Figure 126. Alternate Simplified Power Supply Configuration

OUTLINE DIMENSIONS

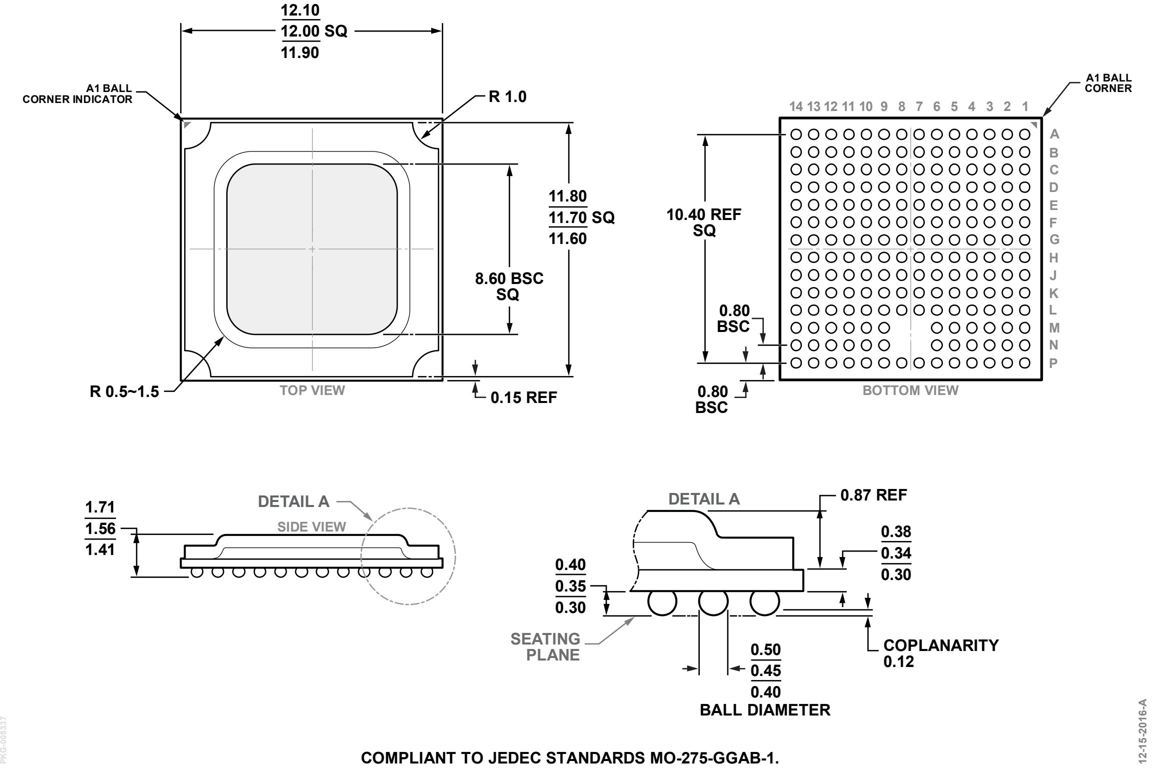


Figure 127. 192-Ball Ball Grid Array, Thermally Enhanced [BGA_ED] (BP-192-1) Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range[2]	Package Description	Package Option
AD9213BBPZ-6G	−20°C to +115°C	192-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]	BP-192-1
AD9213BBPZ-10G	−20°C to +115°C	192-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]	BP-192-1
AD9213-6GEBZ		Evaluation Board	
AD9213-10GEBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

[2] Specified operating junction temperature (T_J). Startup at T_J = −40°C is guaranteed.