

ESD9R3.3S, SZESD9R3.3S

ESD Protection Diode Ultra-Low Capacitance

The ESD9R is designed to provide ESD protection for ASSPs and ASICs used in ultra low current applications such as human body sensors. These devices have been designed for leakage under 1 nA from 0°C to 50°C when turned off. During an ESD event, these devices turn on to clamp the ESD to a safe voltage level for the IC. These devices have the added benefits of low capacitance for high speed data lines and small package size for space constrained designs.

Specification Features:

- Ultra-Low Leakage < 1 nA
- Ultra-Low Capacitance 0.5 pF
- Low Clamping Voltage
- Small Body Outline Dimensions:
0.039" x 0.024" (1.00 mm x 0.60 mm)
- Low Body Height: 0.016" (0.4 mm)
- Stand-off Voltage: 3.3 V
- Response Time < 1.0 ns
- IEC61000-4-2 Level 4 ESD Protection
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free and Halogen-Free Device

Mechanical Characteristics:

CASE: Void-free, transfer-molded, thermosetting plastic
Epoxy Meets UL 94 V-0

LEAD FINISH: 100% Matte Sn (Tin)

MOUNTING POSITION: Any

QUALIFIED MAX REFLOW TEMPERATURE: 260°C

Device Meets MSL 1 Requirements

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|------------------|-------------------|------|
| IEC 61000-4-2 (ESD) Contact Air HBM | | ±10 ±15 ±16 | kV |
| Total Power Dissipation on FR-5 Board (Note 1) @ T _A = 25°C | P _D | 150 | mW |
| Storage Temperature Range | T _{stg} | -55 to +150 | °C |
| Junction Temperature Range | T _J | -55 to +125 | °C |
| Lead Solder Temperature - Maximum (10 Second Duration) | T _L | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-5 = 1.0 x 0.75 x 0.62 in.

See Application Note AND8308/D for further description of survivability specs.



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SOD-923
CASE 514AB

MARKING DIAGRAM



J = Specific Device Code
M = Date Code

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|----------------------|--------------------|
| ESD9R3.3ST5G | SOD-923 (Pb-Free) | 8000 / Tape & Reel |
| SZESD9R3.3ST5G | SOD-923 (Pb-Free) | 8000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DEVICE MARKING INFORMATION

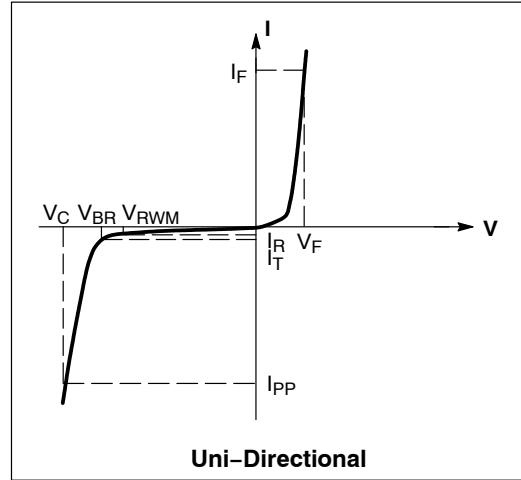
See specific marking information in the device marking column of the Electrical Characteristics tables starting on page 2 of this data sheet.

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ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter |
|-----------|--|
| I_{PP} | Maximum Reverse Peak Pulse Current |
| V_C | Clamping Voltage @ I_{PP} |
| V_{RWM} | Working Peak Reverse Voltage |
| I_R | Maximum Reverse Leakage Current @ V_{RWM} |
| V_{BR} | Breakdown Voltage @ I_T |
| I_T | Test Current |
| I_F | Forward Current |
| V_F | Forward Voltage @ I_F |
| P_{pk} | Peak Power Dissipation |
| C | Max. Capacitance @ $V_R = 0$ and $f = 1.0$ MHz |



*See Application Note AND8308/D for detailed explanations of datasheet parameters.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted, $V_F = 1.0$ V Max. @ $I_F = 10$ mA for all types)

| Device* | Device Marking | V_{RWM} (V) | I_R (nA) @ 1 V $T_A = 0^\circ\text{C}$ to 50°C (Note 4) | V_{BR} (V) @ I_T (Note 2) | I_T | C (pF) | | V_C (V) @ $I_{PP} = 1$ A (Note 5) | V_C |
|--------------|----------------|---------------|--|----------------------------------|-------|--------|-----|---|------------------------------|
| | | Max | Max | Min | mA | Typ | Max | Max | Per IEC61000-4-2 (Note 3) |
| ESD9R3.3ST5G | J** | 3.3 | 1.0 | 4.8 | 1.0 | 0.5 | 0.9 | 7.8 | Figures 1 and 2 See Below |

*Includes SZ-prefix device where applicable.

**Rotated 270° .

- V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C .
- For test procedure see Figures 3 and 4 and Application Note AND8307/D.
- Limits over temperature are guaranteed by design, not production tested.
- V_C measured using pulse waveform in Figure 5.

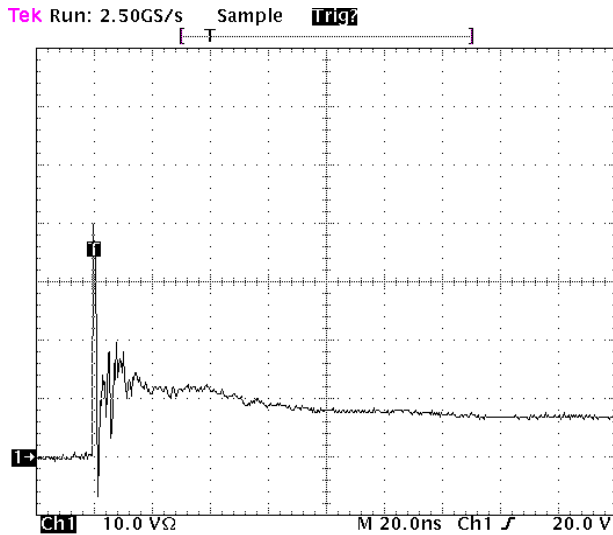


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2

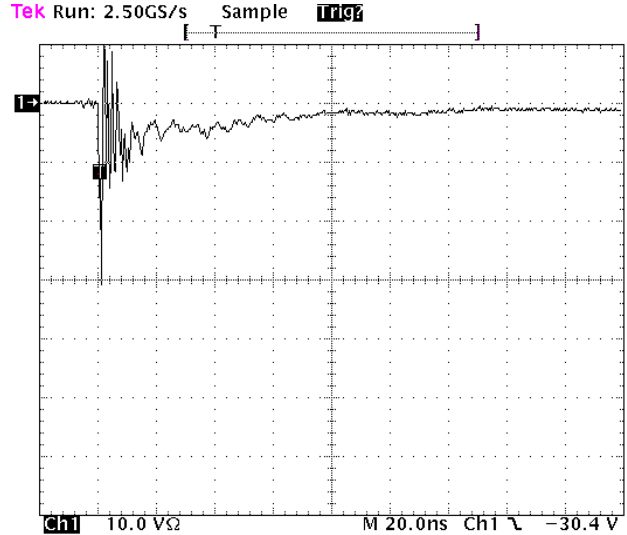


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2

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IEC 61000-4-2 Spec.

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|-------|-------------------|------------------------|----------------------|----------------------|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |



Figure 3. IEC61000-4-2 Spec

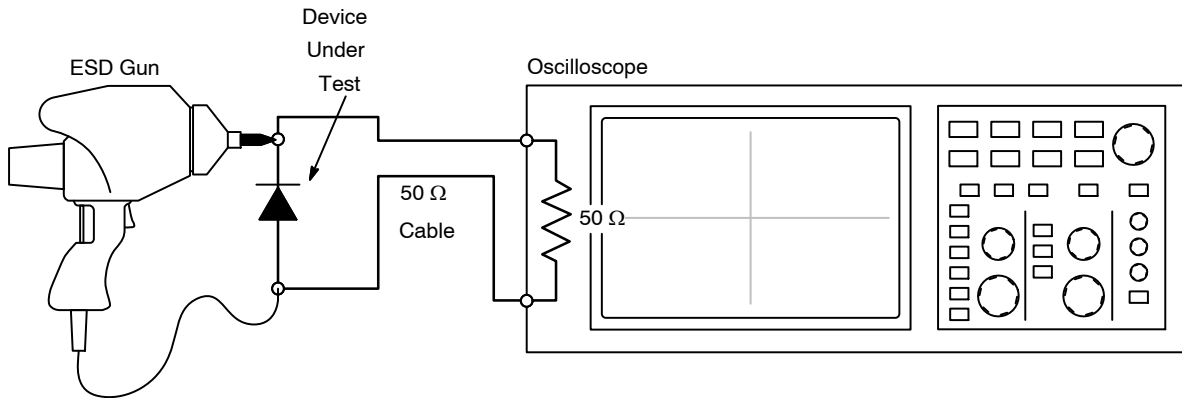


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

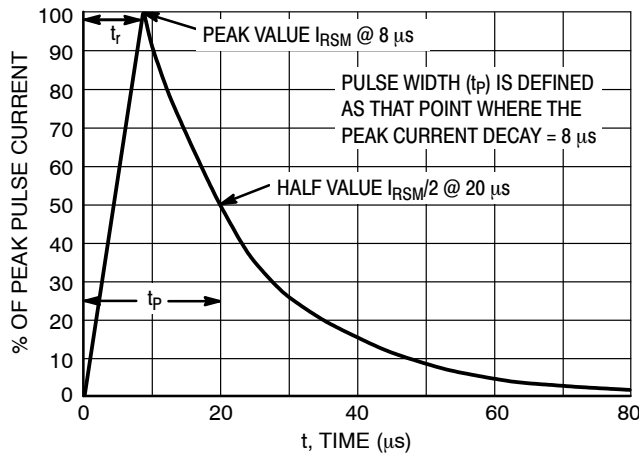


Figure 5. 8 x 20 μs Pulse Waveform

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