The most recent version of this page is at Rev. 30 Aug 2022 20:19 by Jessy Kaufman. Jump to the Previous approved version 24 Mar 2021 01:35 by avalente.

This is an old revision of the document!

Quick Start Guide for Testing the AD9213 Customer Evaluation Board AD9213-100EBZ-B Using the ADS8-V1EBZ FPGA-Based Capture Board

Typical Setup

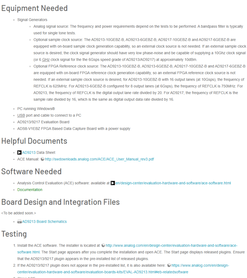


Figure 1 AD9213-100EBZ-B Evaluation Board and ADS8-V1EBZ Data Capture Board, default configuration with external clocks

Configuration for External Clocks

New photos and information here

Equipment Needed

- Signal Generators
  - Analog signal source: The frequency and power requirements depend on the tests to be performed. A bandpass filter is typically used for single tone tests.
  - Optional sample clock source: The AD9213-100EBZ-B, AD9213-80EBZ-B, AD9217-105EBZ-B and AD9217-80EBZ-B are equipped with on-board sample clock generation capability, so an external clock source is not needed. If an external sample clock source is desired, the clock signal generator should have very low phase noise and be capable of supplying a 10Dbm clock signal into a 50Ω clock input (see the Clock Configuration section of the AD9213/AD9217 data sheet).
  - Optional FPGA Reference clock source: The AD9213-100EBZ-B, AD9213-80EBZ-B, AD9217-105EBZ-B and AD9217-80EBZ-B are equipped with on-board FPGA reference clock generation capability, so an external FPGA reference clock source is not needed. If an external sample clock source is desired, for AD9213-105EBZ-B with 1% output lanes (at 1Gbps), the frequency of REFCLK is 625MHz. For AD9213-80EBZ-B configured for 4-output lanes (at 6Gbps), the frequency of REFCLK is 750MHz. For AD9217, the frequency of REFCLK is the digital output lane rate divided by 20. For AD9237, the frequency of REFCLK is the sample rate divided by 16, which is the same as digital output data rate divided by 16.
- PC, running Windows®
- USB port and cable to connect to a PC
- ADIS7105/7 Evaluation Board
- ADS8-V1EBZ FPGA-Based Data Capture Board with a power supply

Helpful Documents

- AD9213 Data Sheet
- ACE Manual, http://wiki.analog.com/ACE/ACE_User_Manual_rev3.pdf

Software Needed

- Analysis Control Evaluation (ACE) software available at https://engineerzone.analog.com/ace
- Documentation

Board Design and Integration Files

<To be added soon>

- Schematics
  - AD9213 Board Schematics

Testing

1. Install the ACE software. The installer is located at https://www.analog.com/en/design-center/evaluation-hardware-and-software/ace-software.html. The Start page appears after you complete the installation and open ACE. The Start page displays released plugins. Ensure that the AD9213/9217 plugin appears in the pre-installed list of released plugins.
2. If the AD9213/9217 plugin does not appear in the pre-installed list, it is also available here: https://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/EVAL-AD9213.html#eb-relatedsoftware
3. Close ACE.
4. Install jumper on P3 as shown below:

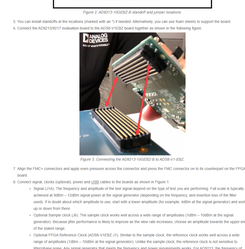


Figure 2 AD9213-100EBZ-B standoff and jumper locations

5. You can install standoffs at the locations marked with an "S" if needed. Alternatively, you can use foam sheets to support the board.
6. Connect the AD9213/9217 evaluation board to the ADS8-V1EBZ board together as shown in the following figure.

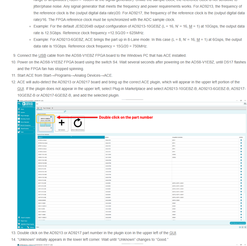
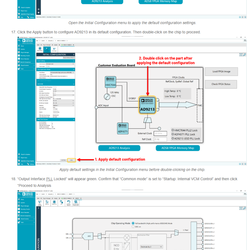
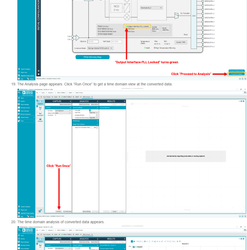


Figure 3 Connecting the AD9213-100EBZ-B to ADS8-V1EBZ

7. Align the FMC+ connectors and apply even pressure across the connector and press the FMC connector on to its counterpart on the FPGA board.
8. Connect signal, clocks (optional), power and USB cables to the boards as shown in Figure 1.
   - Signal (J1): The frequency and amplitude of the input signal depend on the type of test you are performing. Full scale is typically achieved at 8dBm. –12dBm signal power at the signal generator (depending on the frequency, and insertion loss of the filter used). If in doubt about what amplitude to use, start with a lower amplitude (for example, -40Bm at the signal generator) and work up or down from there.
   - Optional Sample clock (J4): The sample clock works well across a wide range of amplitudes (+2dBm – +10dBm at the signal generator). Because jitter performance is likely to improve as the sine -ple increases, choose an amplitude towards the upper end of the stated range.
   - Optional FPGA Reference Clock (J3/J6 FPGA REFCLK): Similar to the sample clock, the reference clock works well across a wide range of amplitudes (+2dBm – +10dBm at the signal generator). Because jitter performance is likely to improve as the amplitude increases (Rectilinear noise), also typical generators that meets the frequency and power requirements works. For AD9213, the frequency of the reference clock is the output digital data rate/n20. For AD9217, the frequency of the reference clock is the output digital data rate/n16. The FPGA reference clock must be synchronized with the ADC sample clock.
   - Example: For the default JESD204B output configuration of AD9213-105EBZ (L = 10, M = 10, N' = 16, S = 1), at 1Gsps, the output data rate is 10 Gbps. Therefore, the reference clock = 10 Gbps/20 = 625MHz
   - Example: For AD9213-80EBZ, ACE brings the part up in 6-Lane mode. In this case (L = 6, M = 10, N' = 16, S = 1) at 6Gsps, the output data rate is 10Gbps. Reference clock frequency = 10Gbit = 750MHz
9. Connect the USB cable from the ACE8-V1EBZ FPGA board to the Windows PC that has ACE installed.
10. Power on the ACE8-V1EBZ FPGA board using the switch. Wait several seconds after powering on the ACE8-V1EBZ. LED0, LED1 flashes and the FPGA fan has stopped spinning.
11. Start ACE from Start>>Programs>>Analog Devices>>ACE.
12. ACE will auto-detect the AD9213 or AD9217 board and bring up the correct ACE plugin, which will appear in the upper left portion of the GUI. If the plugin does not appear in the upper left, see the Plug-In Marketplace and select AD9213-105EBZ-B, AD9213-80EBZ-B, AD9217-105EBZ-B or AD9217-80EBZ-B, and add the selected plugin.

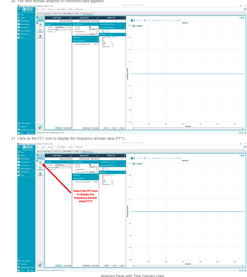


13. Double click on the AD9213 or AD9217 part number in the plugin icon in the upper left of the GUI.
14. "Unknown" initially appears in the lower left corner. Wait until "Unknown" changes to "Good."



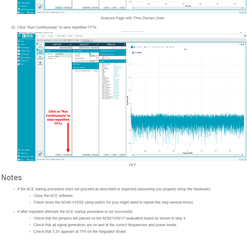
AD9213/9217 board view

15. After "Status=Good" appears in the lower left, turn on the signal generators for the clock, reference clock, and signal.
16. Open the menu "Initial Configuration"



Open the Initial Configuration menu to apply the default configuration settings

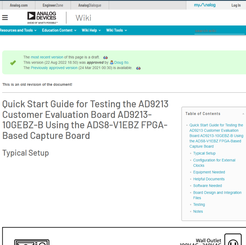
17. Click the Apply button to configure AD9213 or its default configuration. Then double-click on the chip to proceed



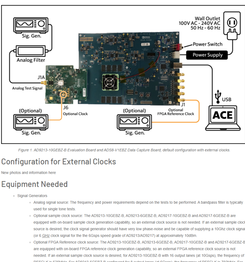
Apply default settings in the Initial Configuration menu, before double-clicking on the chip.

18. "Output Interface PLL Locked" will appear green. Confirm that "Common mode" is set to "Startup. Internal VCM Control" and then click "Proceed to Analysis"

19. The Analysis page appears. Click "Run Once" to get a time domain view at the converted rates.



20. The time domain analysis of converted data appears.



21. Click on the FFT icon to display the frequency domain view (FFT).

Analysis Page with Time Domain Data

22. Click "Run Continuously" to view repetitive FFTs.

FFT

Notes

- If the ACE startup procedure does not proceed as described or expected (assuming you properly setup the hardware):
  - Close the ACE software
  - Power down the ADS8-V1EBZ using switch S4 (you might need to inject the step several times).
- If after repeated attempts the ACE startup procedure is not successful:
  - Check that the jumpers are placed on the AD9213/9217 evaluation board as shown in step 4.
  - Check that all signal generators are on and at the correct frequencies and power levels.
  - Check that 3.3V appears at TP9 on the Regulator Board.

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