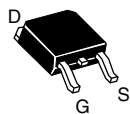
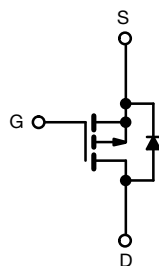


Power MOSFET

DDAK
(TO-252)

IPAK
(TO-251)


P-Channel MOSFET

FEATURES

- Advanced process technology
- Fully avalanche rated
- Surface-mount (IRFR9214, SiHFR9214)
- Straight lead (IRFU9214, SiHFU9214)
- P-channel
- Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

DESCRIPTION

Third generation power MOSFETs from Vishay utilize advanced processing techniques to achieve low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU, SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface-mount applications.

PRODUCT SUMMARY

V _{DS} (V)	-250	
R _{DS(on)} (Ω)	V _{GS} = -10 V	3.0
Q _g (Max.) (nC)	14	
Q _{gs} (nC)	3.1	
Q _{gd} (nC)	6.8	
Configuration	Single	

ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and halogen-free	SiHFR9214-GE3	SiHFR9214TRL-GE3	SiHFR9214TR-GE3	SiHFU9214-GE3
Lead (Pb)-free	IRFR9214PbF	IRFR9214TRLPbF ^a	IRFR9214TRPbF ^a	IRFU9214PbF

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	-250	V
Gate-source voltage	V _{GS}	± 20	
Continuous drain current	V _{GS} at -10 V	T _C = 25 °C	A
		T _C = 100 °C	
Pulsed drain current ^a	I _{DM}	-11	
Linear derating factor		0.40	W/°C
Single pulse avalanche energy ^b	E _{AS}	100	mJ
Repetitive avalanche current ^a	I _{AR}	-2.7	A
Repetitive avalanche energy ^a	E _{AR}	5.0	mJ
Maximum power dissipation	P _D	50	W
Peak diode recovery dV/dt ^c	dV/dt	-5.0	V/ns
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^d	For 10 s	260	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting T_J = 25 °C, L = 27 mH, R_g = 25 Ω, I_{AS} = -2.7 A (see fig. 12)
- I_{SD} ≤ -2.7 A, dI/dt ≤ 600 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	-	110	°C/W
Maximum junction-to-ambient (PCB mount) ^a	R_{thJA}	-	-	50	
Maximum junction-to-case (drain)	R_{thJC}	-	-	2.5	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA		- 250	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = - 1 mA		-	- 0.25	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA		- 2.0	-	- 4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = - 250 V, V _{GS} = 0 V		-	-	- 100	μA
		V _{DS} = - 200 V, V _{GS} = 0 V, T _J = 125 °C		-	-	- 500	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = - 10 V	I _D = - 1.7 A ^b	-	-	3.0	Ω
Forward transconductance	g _{fs}	V _{DS} = - 50 V, I _D = - 1.7 A		0.9	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = - 25 V, f = 1.0 MHz, see fig. 5		-	220	-	pF
Output capacitance	C _{oss}			-	75	-	
Reverse transfer capacitance	C _{rss}			-	11	-	
Total gate charge	Q _g	V _{GS} = - 10 V	I _D = - 1.7 A, V _{DS} = - 200 V, see fig. 6 and 13 ^b	-	-	14	nC
Gate-source charge	Q _{gs}			-	-	3.1	
Gate-drain charge	Q _{gd}			-	-	6.8	
Turn-on delay time	t _{d(on)}	V _{DD} = - 125 V, I _D = - 1.7 A, R _g = 21 Ω, R _D = 70 Ω, see fig. 10 ^b		-	11	-	ns
Rise time	t _r			-	14	-	
Turn-off delay time	t _{d(off)}			-	20	-	
Fall time	t _f			-	17	-	
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal source inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	- 2.7	A
Pulsed diode forward current ^a	I _{SM}			-	-	- 11	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = - 2.7 A, V _{GS} = 0 V ^b		-	-	- 5.8	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = - 1.7 A, dI/dt = 100 A/μs ^b		-	150	220	ns
Body diode reverse recovery charge	Q _{rr}			-	870	1300	nC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

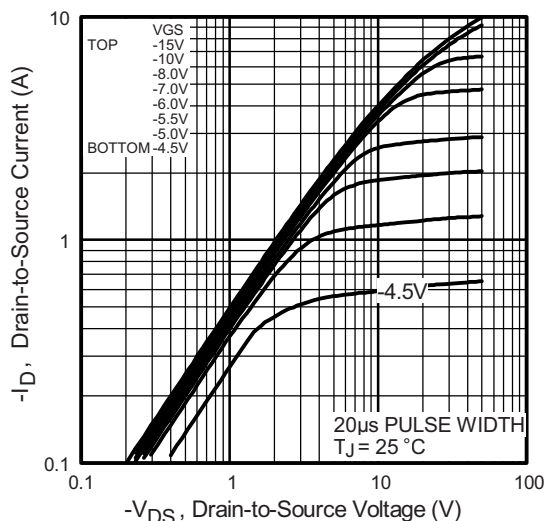


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

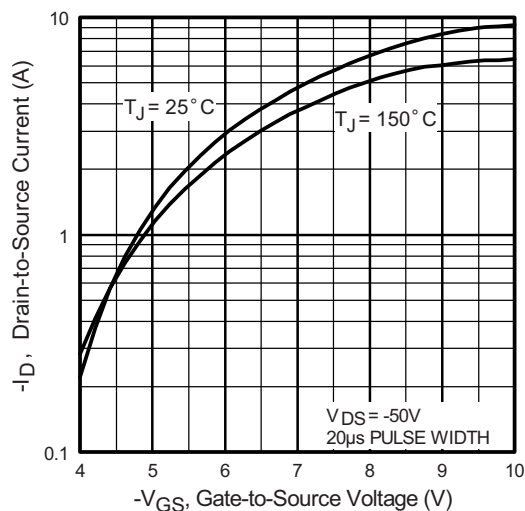


Fig. 2 - Typical Transfer Characteristics

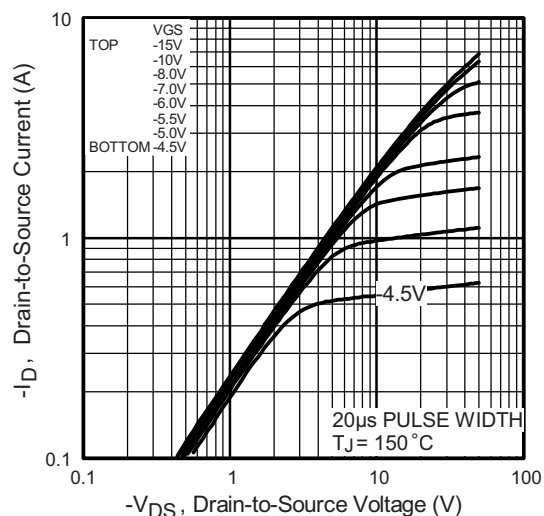


Fig. 1 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

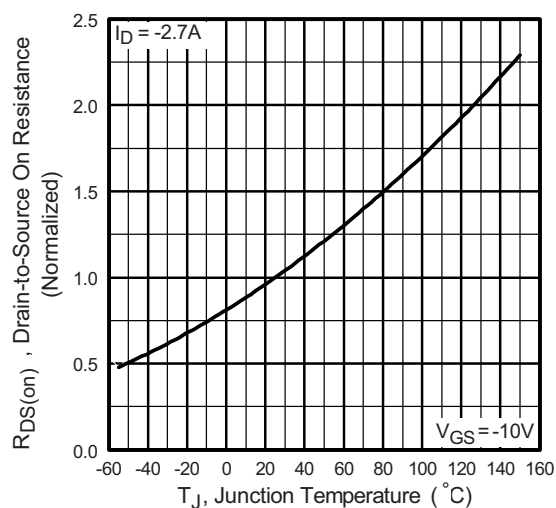
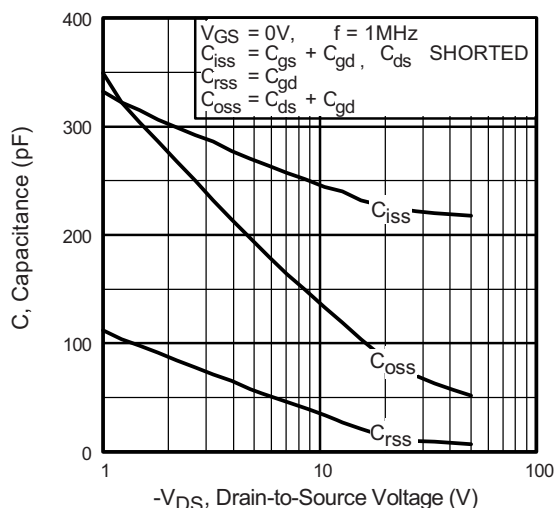
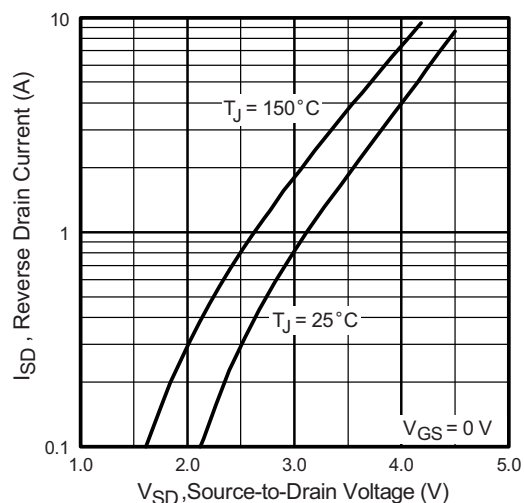
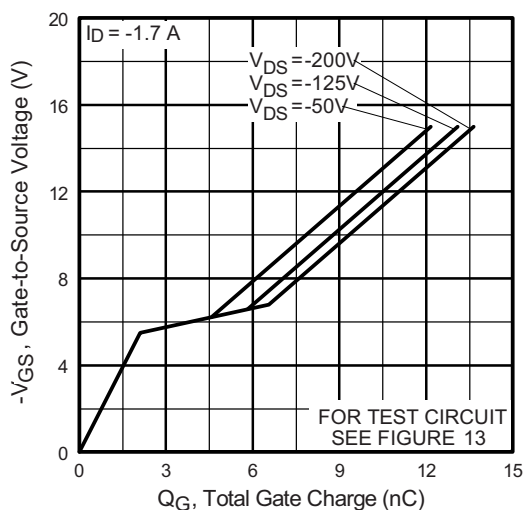
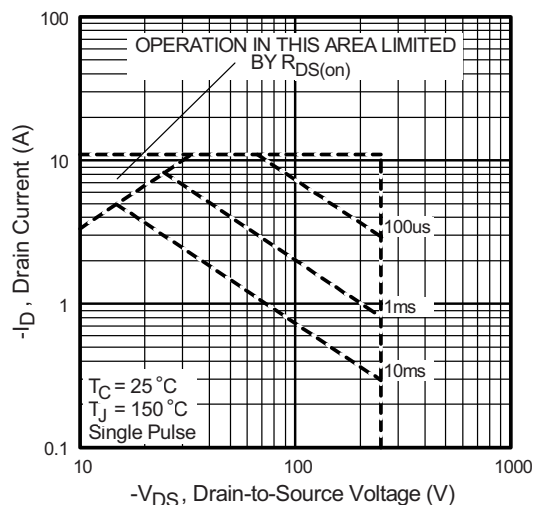


Fig. 3 - Normalized On-Resistance vs. Temperature


Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 6 - Typical Source-Drain Diode Forward Voltage

Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 7 - Maximum Safe Operating Area

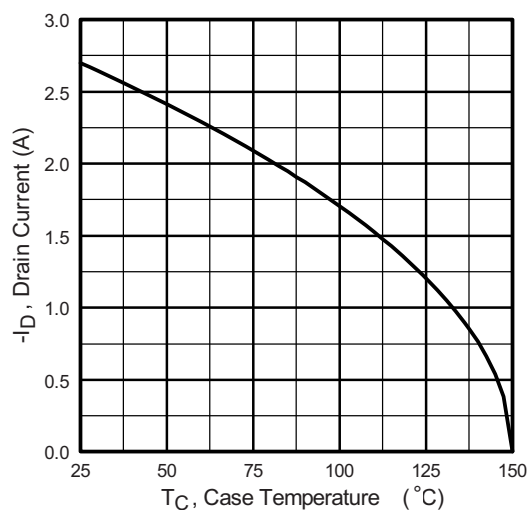


Fig. 8 - Maximum Drain Current vs. Case Temperature

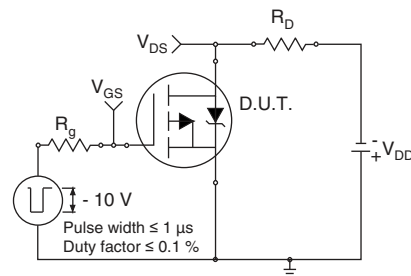


Fig. 10a - Switching Time Test Circuit

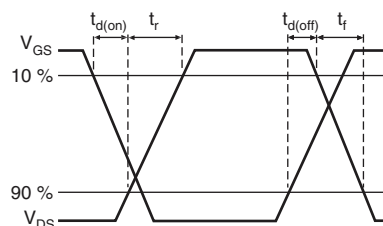


Fig. 10b - Switching Time Waveforms

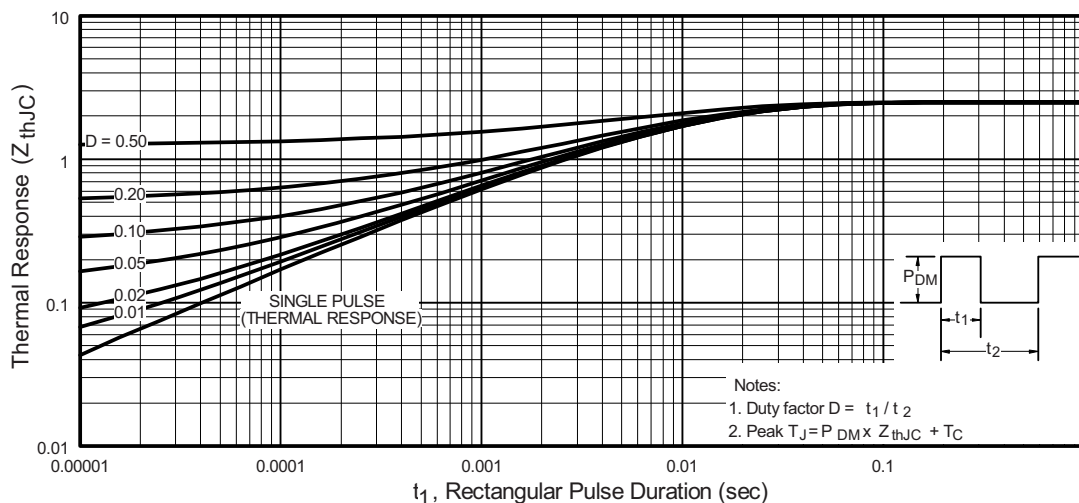


Fig. 9 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

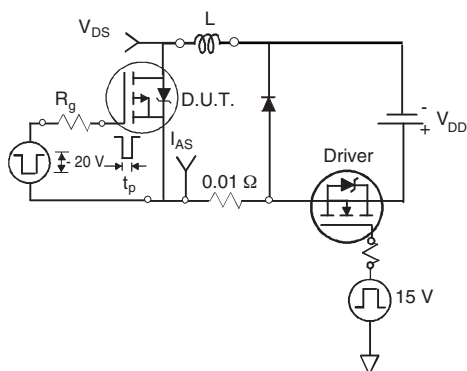

Fig. 12a - Unclamped Inductive Test Circuit

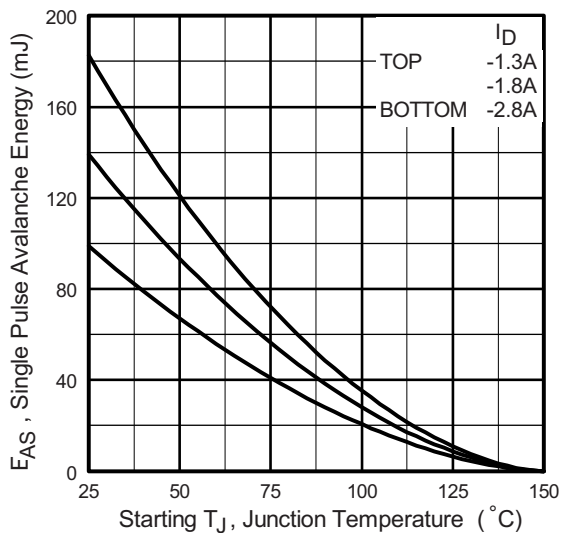
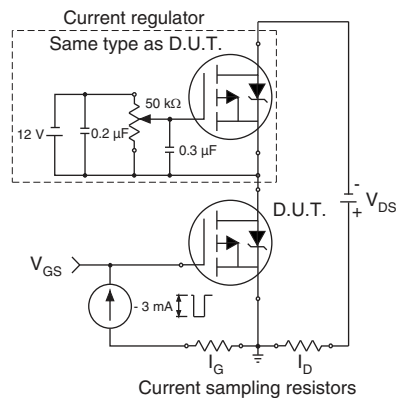
Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

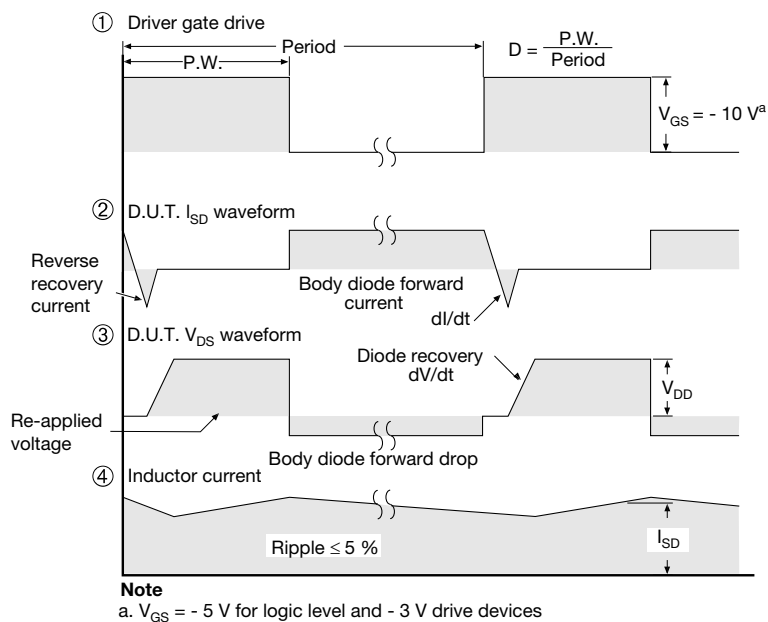


Fig. 10 - For P-Channel

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TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



DIM.	MILLIMETERS	
	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

DIM.	MILLIMETERS	
	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ_1	0°	15°
θ_2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E22-0399-Rev. R, 03-Oct-2022
DWG: 5347

Case Outline for TO-251AA (High Voltage)

OPTION 1:



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
θ1	0°	15°	0°	15°
θ2	25°	35°	25°	35°

ECN: E21-0682-Rev. C, 27-Dec-2021
DWG: 5968

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension are shown in inches and millimeters
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- Thermal pad contour optional with dimensions b4, L2, E1 and D1
- Lead dimension uncontrolled in L3
- Dimension b1, b3 and c1 apply to base metal only
- Outline conforms to JEDEC® outline TO-251AA



OPTION 2: FACILITY CODE = N



DIM.	MIN.	NOM.	MAX.
A	2.180	2.285	2.390
A1	0.890	1.015	1.140
b	0.640	0.765	0.890
b1	0.640	0.715	0.790
b2	0.760	0.950	1.140
b3	0.760	0.900	1.040
b4	4.950	5.205	5.460
c	0.460	-	0.610
c1	0.410	-	0.560
c2	0.460	-	0.610
D	5.970	6.095	6.220
D1	4.300	-	-

DIM.	MIN.	NOM.	MAX.
D2	5.380	-	-
E	6.350	6.540	6.730
E1	4.32	-	-
e	2.29 BSC		
L	8.890	9.270	9.650
L1	1.910	2.100	2.290
L2	0.890	1.080	1.270
L3	1.140	1.330	1.520
L4	1.300	1.400	1.500
theta1	0°	7.5°	15°
theta2	4°	-	-

ECN: E21-0682-Rev. C, 27-Dec-2021
DWG: 5968

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- All dimension are in millimeters, angles are in degrees
- Heat sink side flash is max. 0.8 mm

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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